Start Here Guide
for the HDL Designer Series™

Software Version 2010.3

June, 2011

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Send Feedback on Documentation: supportnet.mentor.com/user/feedback_form.cfm

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Chapter 1
Introduction

The HDL Designer Series

The **HDL Designer Series** ™ (HDS) is a family of tools for electronic system design which fully support the VHDL and Verilog hardware description languages.

The HDL Designer Series design environment helps you to manage the complexity of growing ASIC and FPGA designs by providing:

- A predictable and flexible design process
- Rapid design development
- Practical intellectual property and design reuse
- Powerful design analysis
- Automated design communications

For full information about the HDL Designer Series including brochures, datasheets and a product feature configuration matrix visit the Web site:

`http://www.mentor.com/hdldesigner/`

HDL Author

The **HDL Author** ™ tool is based on a design manager which provides an advanced environment for HDL design creation and the management of complex hierarchical designs.

The design manager provides design management facilities including a project manager, multiple design explorers, version management interfaces, template and task managers.

The project manager allows you to manage the library mapping that specifies the location of your design data. Projects can be created or modified and stored as individual user or shared team resources.

You can open multiple design explorers to display your design data as design units, HDL files or logical design objects. The full design hierarchy beneath any design object can be explored in a separate hierarchy subwindow. Additional subwindows can be used to explore source design side data and downstream data.

The version management interface supports the GNU Revision Control System (RCS), GNU Concurrent Versions System (CVS), Rational ClearCase, Synchronicity DesignSync, Cliosoft SoS and the Microsoft or Mainsoft Visual SourceSafe version control systems. RCS and CVS are included in the distribution or the other systems can be selected when they are available on your file system.

The task manager supports customizable interfaces to downstream tools and design flows. Default tasks are provided to support the generation of HDL from graphical source views and compilation, simulation or synthesis using a range of industry standard tools.

The default tasks include interfaces for the Model*Sim*®, Cadence NC-Sim and Synopsys VCS or VCSi simulators, LeonardoSpectrum™, Precision® Synthesis, Synopsys Design Compiler or Synplify synthesis tools, Altera MegaWizard, Xilinx CORE generator and Atrenta SpyGlass design rule checker. The tasks are defined using Tcl (tool control language) which can be copied or modified to create your own custom tool or to run an external program or Tcl script.

The template manager provides default templates for HDL text views which can be edited to support your local design standards including multiple alternative templates for each view type.

The design manager supports tasks and templates maintained by each individual user and as shared team resources maintained by a team administrator.

The design manager includes an integrated **DesignPad** language sensitive text editor for the creation and maintenance of HDL text designs or can be configured to use a range of supported external text editors.

Graphical design is supported by tabular IO and graphical symbol interface editors. The interconnections between design units in a hierarchical design can be maintained using a graphical block diagram editor or in tabular format using an interface-based design™ (IBD) view. Leaf-level views can be defined using HDL text views or using the state diagram, flow chart and truth table editors which allow an entire design to be represented graphically.

Existing HDL designs can be imported into the HDL Designer Series data model while preserving any file structure and design data integrity.

Any text or graphical view can be printed or (on Windows only) directly included in a documentation tool using object linking and embedding (OLE).

A **ModuleWare** library provides a range of standard components which can be instantiated in a graphical or HDL text design (when you are using the DesignPad editor).

A simulation analyzer interface provides error cross-referencing and animation facilities to assist with design debug operations. Full debug support is provided for the ModelSim or Cadence NC-Sim simulator tasks but invocation only for Synopsys VCS or VCSi.

HDL Designer

The **HDL Designer** ™ tool includes the facilities provided by **HDL Author**. In addition, it is a visualization and debug tool including **HDL2Graphics** ™ which can import any complete or partial HDL text based design and convert the design into a hierarchy of graphical or tabular views. The design structure can be represented as graphical block diagrams or tabular IBD views. Primitive leaf-level views can be viewed as state diagram, flow chart or HDL text views.

Non-logical changes can be made to any graphical view and they can be printed or exported as HTML Web pages for use in design documentation. On Windows systems, graphical views can be directly included in a documentation tool using the object linking and embedding (OLE) feature.

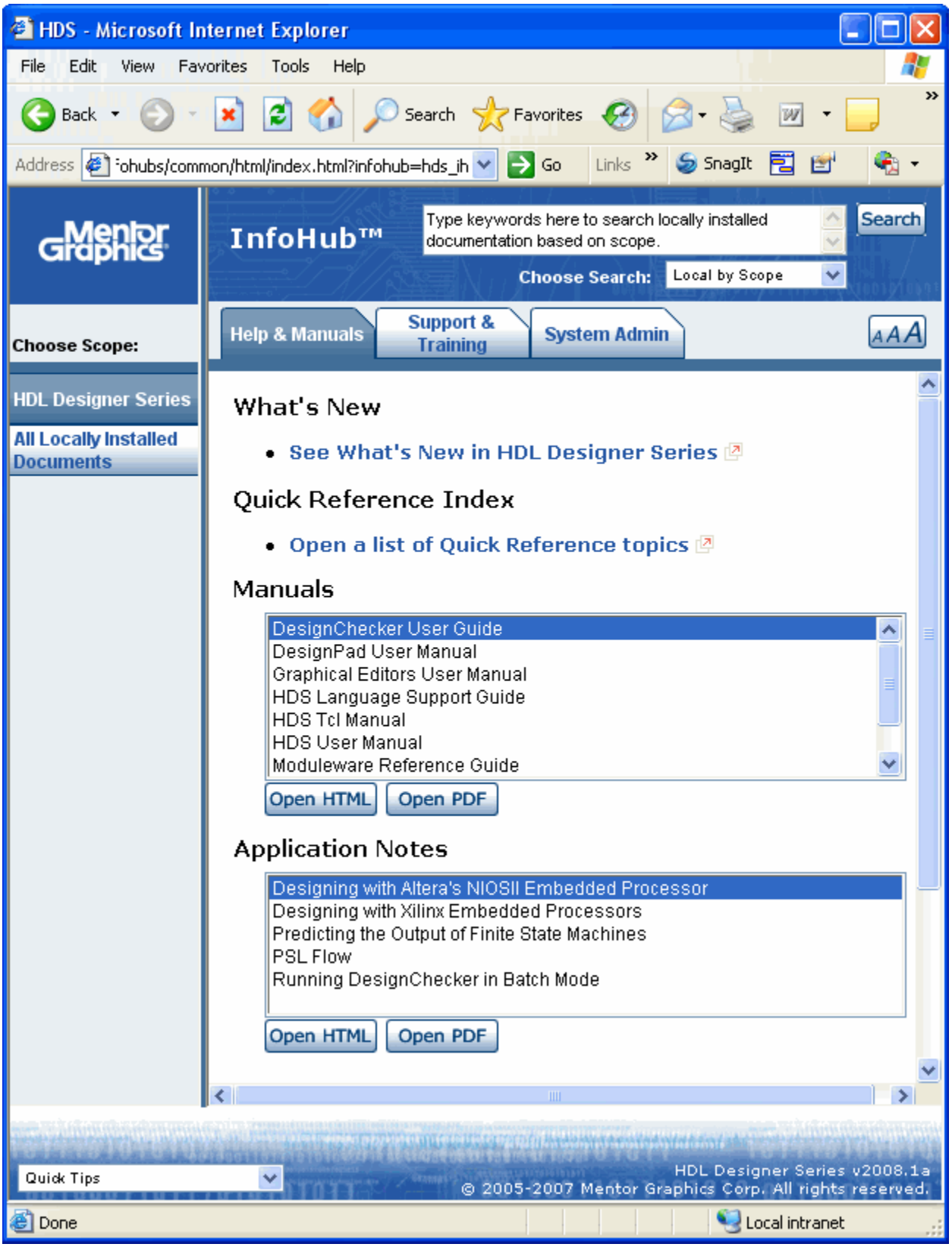
Version management is available for your imported HDL text and rendered graphical views.

Design explorers can be used to explore the relationship between design units. However, design management operations and logical edits which would modify design behavior are disabled.

Documentation

The HDL Designer Series documentation (including this guide) can be accessed through the InfoHub, which is opened by selecting **Help and Manuals** from the **Help** menu found in any of the application windows.

The InfoHub is the Mentor Graphics information center. From the InfoHub, you can access all locally installed HDL Designer Series documentation, release management information, and tutorials. The InfoHub also provides direct access to SupportNet site to check for software updates, technical notes, and application notes.


HDS - Microsoft Internet Explorer
File Edit View Favorites Tools Help
Back Search Favorites
Address ohubs/common/html/index.html?infohub=hds_ih
Go Links SnagIt
InfoHub™
Type keywords here to search locally installed documentation based on scope.
Search
Choose Search: Local by Scope
Choose Scope:
HDL Designer Series
All Locally Installed Documents
Help & Manuals
Support & Training
System Admin
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See What's New in HDL Designer Series
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Manuals
DesignChecker User Guide
DesignPad User Manual
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HDS Language Support Guide
HDS Tcl Manual
HDS User Manual
Moduleware Reference Guide
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Application Notes
Designing with Altera's NIOSII Embedded Processor
Designing with Xilinx Embedded Processors
Predicting the Output of Finite State Machines
PSL Flow
Running DesignChecker in Batch Mode
Open HTML
Open PDF
Quick Tips
HDL Designer Series v2008.1a
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Done
Local intranet

The HDS InfoHub mainly comprises of the following tabs:

- Help and Manuals
- Support and Training
- System Admin

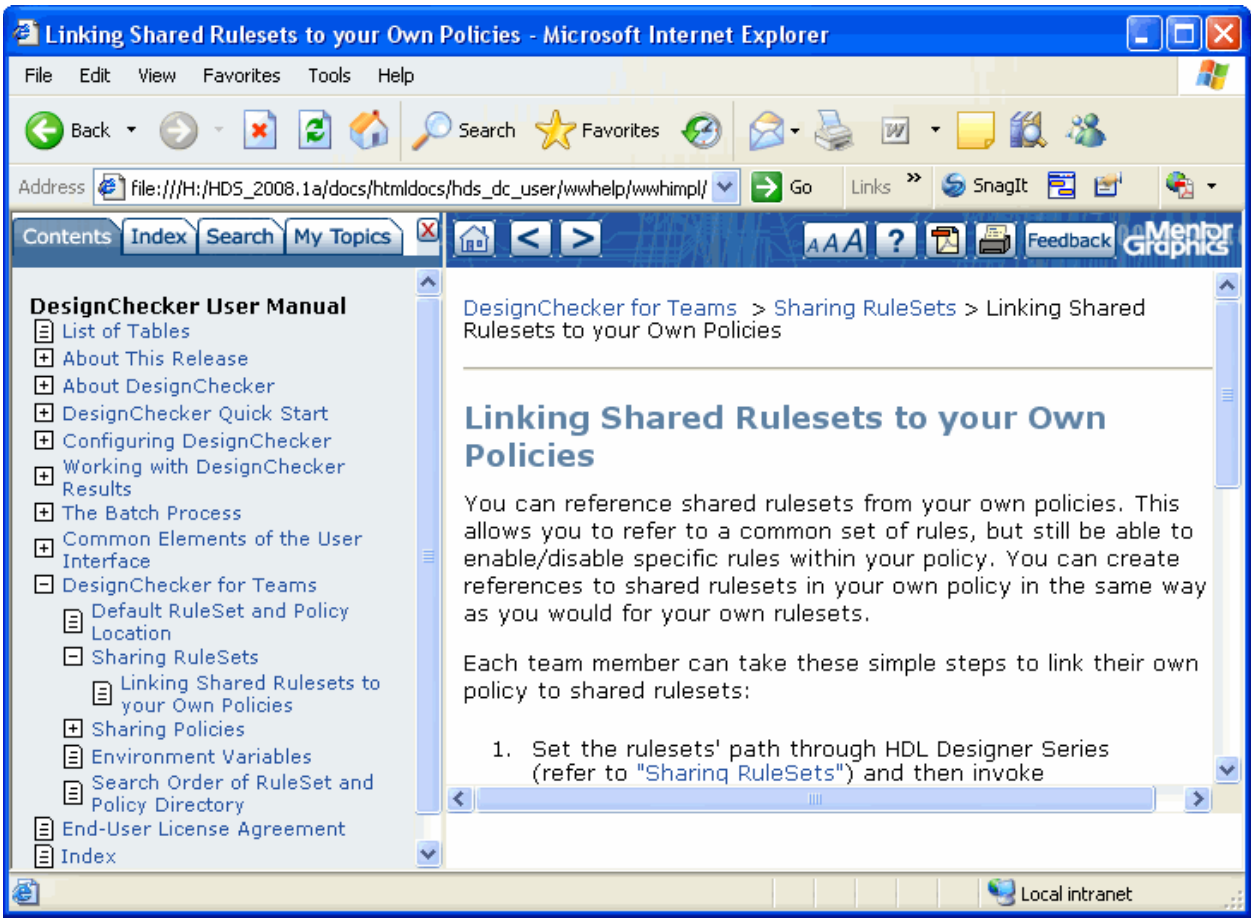
Note

The Quick Tips dropdown list on the lower left side of the InfoHub provides useful information on the InfoHub and how to use it efficiently. For example, it includes a list of supported browsers, essential browser settings, the method of adding custom tabs to the InfoHub, and so on.

Help and Manuals

This tab provides all the documents covering the different editors in HDL Designer Series. To open a document, select the required document, and then click on one of the following buttons:

- **Open HTML —** opens an HTML version of the document for browsing.



The HTML page has a navigation pane on the left hand side consisting of the Contents, Index and Search tabs through which you can navigate through the document, in addition to a tab titled My Topics.

- Content — this tab has a list of all the topics available in the opened document.
- Index — this tab has a number of alphabetically ordered keywords. You can view the index of the current opened document only or all the installed documents. If you have a Search List created, you can choose to view the indexes of all the documents it contains.
- Search — this tab enables you to search the current opened document only, all installed documents, or SupportNet. If you have a Search List created, you can choose to search within its contents.
- My Topics — this tab enables you to bookmark your favorite topics. You can save up to twenty topics from different manuals. To add a topic, make sure you open it first then click Add Topic in the tab. To delete a topic, just click the deletion button next to the topic title.

Note

A Search List is a user-defined list of documents that can be used as a search scope whether when running a search from the Search tab of an HTML document or when running a search from the InfoHub itself. Also, a Search List can be used as a scope when viewing the index.

To create/edit a Search List from the Index or Search tabs, click **Create**/**Edit** next to the "My Search List" option, select the required documents from Edit My Scope dialog box and then click **Save**.

Also, a button bar is available in the topic pane through which you can browse the HTML documentation.

Table 1-1. HTML Button Bar

Button	Description
	Displays the title page of current document.
	Displays previous topic.
	Displays next topic.
	Changes the font size.
	Opens the InfoHub help.
	Opens a PDF version of the document.
	Prints the current topic.
	Sends feedback on documentation.

- **Open PDF —** opens a PDF (Adobe Acrobat portable document format) version of the document for printing.

The documents are categorized as follows: What's New, Quick Reference Index, Manuals, Application Notes, and Other Documents.

What's New

This section includes a link to a list of "What's New" presentations covering the features that have been introduced in various HDL Designer Series releases, starting from release 2003.1 up to the latest release.

Quick Reference Index

This section provides a link to a list of various quick reference topics.

Manuals

The manuals listed in this section are as follows:

- The *HDL Designer Series User Manual* describes general user procedures for the **HDL Author** and **HDL Designer** tools.
- The *Graphical Editors User Manual* describes procedures for using the graphical symbol, tabular IO, block diagram, IBD view, flow chart and truth table editors.
- The *State Machine Editors User Manual* describes procedures for using the state diagram and algorithmic state machine editors.
- The *DesignPad Text Editor User Guide* describes procedures for using the integrated **DesignPad** HDL text editor.
- The *DesignChecker User Guide* describes procedures for using the integrated **DesignChecker** ™ static checker.
- The *ModuleWare Reference Guide* describes a library of HDL model generators which can be instantiated in a design and used to implement a large range of standard logic or arithmetic functions for VHDL or Verilog. Descriptions of each generator in the library in a HTML version of this manual can be accessed directly from each part in the library.
- The *HDL Designer Series Tcl Reference Manual* describes procedures for using the HDS library contents API and HDS Tcl API commands.
- The *HDS Language Support Guide* gives an overview on some of the languages supported by HDL Designer Series.
- The *Start Here Guide for the HDL Designer Series* (this document) which gives you introductory information on the HDL Designer Series tools and describes procedures for invoking them.

Application Notes

The following application notes are available:

- Designing with Altera's NIOSII Embedded Processor
- Designing with Xilinx Embedded Processor
- Predicting the Output of Finite State Machines
- PSL Flow
- Running DesignChecker in Batch Mode

Other Documents

This section includes miscellaneous documents as follows:

- Enscript Manual Pages
- GNU Utilities for Comparing and Using Files
- RCS Manual Pages
- Version Management using CVS

Support and Training

This tab provides links to support and training resources, whether locally installed or on SupportNet. This tab comprises of the following sections:

- Technical Support and Downloads
- Tutorials
- Self-running Demos
- Contact Us

Technical Support and Downloads

This section provides a shortcut to signing-up for SupportPro Newsletter, viewing TechNotes, and viewing AppNotes. It also provides access to the product microsite to get downloads, product information, and patches.

Tutorials

This section provides access to locally installed tutorials which include the following:

- The *Interface-Based Design Tutorial* is an introduction to interface-based design (IBD) for users of the **HDL Author** or **HDL Designer** tools which uses HDL import, tabular IO, an IBD view and ModuleWare parts to capture a VHDL or Verilog text design. Simulation and synthesis design flows are illustrated using the Model*Sim* and LeonardoSpectrum tools.
- The *Design Exploration Tutorial* is an introduction to the **HDL Designer** tool. This tutorial shows how this tool can be used to import an existing VHDL or Verilog text design, visualize the design using graphical views and export these views in HTML format.
- The *DesignChecker Tutorial* is an introduction to the **DesignChecker** tool. This tutorial shows how to configure DesignChecker settings, analyze a design, and investigate the analysis results.

Self-Running Demos

This section includes the following “How to” demos:

- DesignChecker Demos
- Interface-Based Design Demos

Contact Us

This section provides a shortcut to opening a service request, providing feedback on the documentation, and providing access to the list of worldwide sales offices.

System Admin

This tab includes the *Release Notes for the HDL Designer Series* which includes information about new features, the *Release Notes for Licensing Mentor Graphics Software*, and the *Transition Guide for the HDL Designer Series* which includes information about updating from a previous HDL Designer Series release. In addition, this tab contains other installation and licensing references.

Searching Documentation

There are two search tools embedded in the InfoHub:

- A keyword search of locally installed HTML content.
- A comprehensive, natural language search of SupportNet that includes all documentation, release notes, technical notes, and application notes.

The following search methods can be performed:

- **Searching All Installed Documents —** this search applies to all locally installed HTML content. This search can be done either through the InfoHub or through the Search tab of any opened HTML document by typing a search keyword and selecting "All Installed Docs", and then running the search.
- **Searching a Specific Product Area Scope of Documents —** this search narrows the results to the set of documents in the specified InfoHub scope. This search can be done either through the InfoHub or through the Search tab of any opened HTML document by typing a search keyword and selecting "Local by Scope" (in case of the InfoHub) or selecting the scope's radio button (in case of the HTML document), and then running the search.
- **Searching a Custom Set of Documents —** this search applies to the documents you added within your Search List, if you have created one. This search can be done either through the InfoHub or through the Search tab of any opened HTML document by typing a search keyword and selecting "My Search List" option, and then running the search.

Note

A Search List is a user-defined list of documents that can be used as a scope when running a search or viewing the index.

To create/edit a Search List from the InfoHub, in the Choose Search dropdown list select "My Search List", click Edit and select the required documents from Edit My Search Scope dialog box, and then click **Save**.

To create/edit a Search List from the Index or Search tabs, click **Create**/**Edit** next to the "My Search List" option, select the required documents from Edit My Search Scope dialog box, and then click **Save**.

- **Searching a Single Document —** this search applies to a single manual whether it is in HTML or in PDF. In case of an HTML document, open the Search tab, type the search keyword and run the search. In case of a PDF document, use the search method of the Acrobat Reader.
- **Searching SupportNet —** the SupportNet can be searched through the InfoHub itself or through the Search tab of an opened HTML document while setting the SupportNet option.

The Quick Tips dropdown list on the lower left side of the InfoHub contains topics that provide more details on the above search methods.

Dialog Box Help

Most of the **Help** buttons on dialog boxes are linked to single-page mini-PDF files which provide links to other related dialog box descriptions and a direct link to the corresponding section in the user manual.

Customer Support

For information about customer support, please choose **How to obtain support** from the **Support** cascade of the **Help** menu.

If you have a problem with the HDL Designer Series software, you can use the **Generate Support Info** from the **Support** cascade of the **Help** menu to create a text file containing information which may help customer support diagnose the problem.

Chapter 2
Invoking HDL Designer Tools

Invoking on Windows

On Windows, the **HDL Designer Series** tools are normally invoked from shortcuts in the Windows **Start** menu or desktop (which are created during installation):

HDL Author
HDL Designer

These shortcuts invoke the *hdldesigner.exe* executable with an appropriate switch for the licensed configuration you have chosen.

You can also double-click over the executable *hdldesigner.exe* file in the Windows Explorer, explicitly enter *hdldesigner.exe* in the Run dialog box from the **Start** menu or double-click on the icon for any **HDL Designer Series** design object. When invoked in this way, the application attempts to find a valid license and invokes with the configuration supported by that license.

Note

You can also invoke on Windows by double clicking on a recognized HDL Designer Series file type in the Windows explorer. For example, by clicking on a block diagram or IBD view file.

Invoking on UNIX or Linux

When you install **HDL Designer Series** products on UNIX or Linux systems, invoke scripts are created for each tool you selected in the install program as shown in the table below. The scripts and corresponding shortcut links are located in the *bin* subdirectory of your installation.

The invocation commands are summarized in the following table:

Table 2-1. HDS Invocation Commands

Tool	Invoke Script	Shortcut
HDL Author HDL Designer	hdl_author hdl_designer	hdla hds

For example, you can invoke **HDL Author** using either of the commands:

```
<install_dir>/bin/hdl_author
or
<install_dir>/bin/hdla
```

Note

All required environment variables are automatically set within the invoke script and need not be explicitly set if you use these scripts to invoke the tools.

Command Line Switches

Command line switches can be used with any of the invocation commands when you invoke a HDL Designer Series tool from a shell, batch script or Windows shortcut.

Command line switches can be used to run a Tcl command file or to set invoke options. You can display a full list of supported switches by using the -help switch or opening the **Quick Reference Index** from the Help and Manuals tab of the HDS InfoHub. To open the InfoHub, select **Help and Manuals** from the **Help** menu.

The *-teamprefsfile* (or *-teamprefs*) and *-prefsfile* (or *-prefs*) switches are supported to allow migration of the preferences from a previous release.

Refer to “Preferences and Resource Files” in the *Transition Guide for the HDL Designer Series* for information about migrating preference files.

If errors are encountered when you use a command line switch, messages are sent to standard output on UNIX but are not reported on Windows unless you pipe the command output to a file.

Team Member Mode

The HDL Designer Series tools are normally invoked in single-user mode. In this mode, all preferences, tasks and templates are stored in writable resource files as defined in the “Resource Files” appendix in the *HDL Designer Series User Manual*.

Alternatively, you can invoke in team member mode by using the **-team_home** command line switch or the HDS_TEAM_HOME environment variable to specify the location of a shared *hds_team* resources directory.

You can also set team member mode and the location of *hds_team* as preferences in the **General** tab of the Main Settings dialog box as described in the “User and Team Preferences” section of the *HDL Designer Series User Manual*.

In team member mode, the shared team resources are read-only although users with write access permissions can edit these resources by selecting Team Administrator mode.

The team resources include version management settings, generated HDL file naming rules, generation properties, file registration, team tasks, team templates, remote simulation directory location, project synthesis properties and custom code generation scripts.

HDS Setup Assistant Wizard

The HDS Setup Assistant Wizard guides you through the configuration of HDL Designer Series tool.

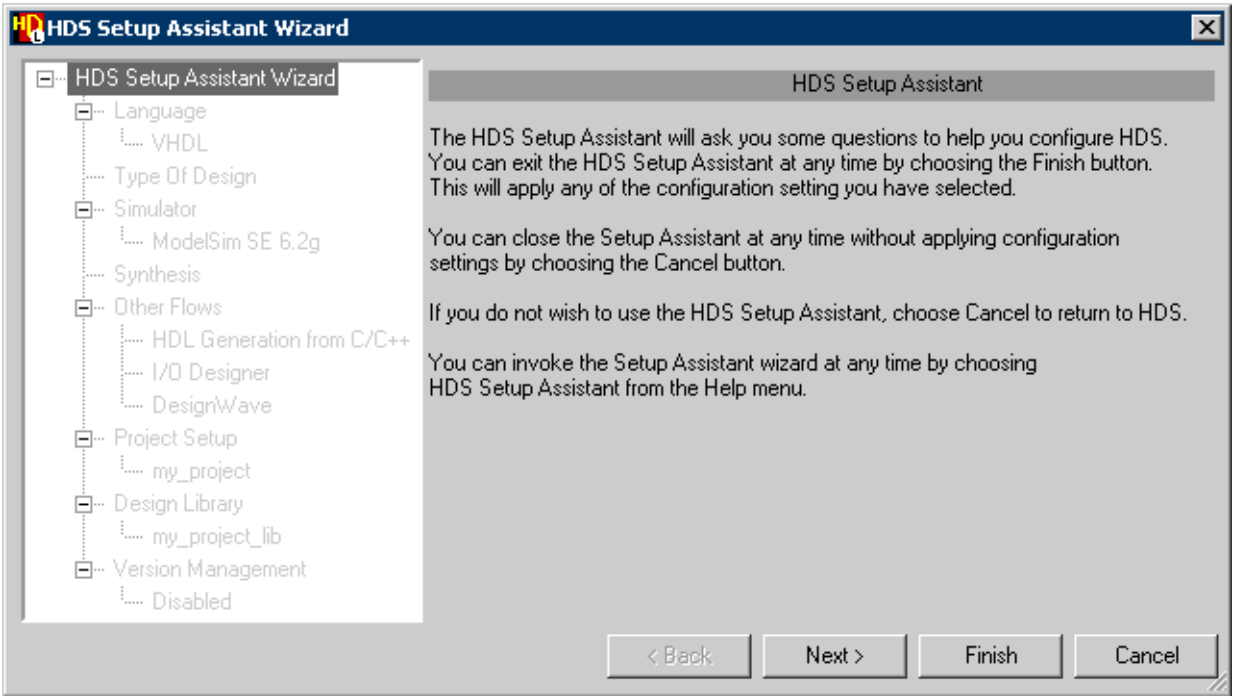
Starting the Wizard

The wizard is started when you invoke a HDL Designer Series tool for the first time. If you choose to cancel the wizard HDS starts with the default examples project, VHDL as the default language and all the available flows and tools.

If you choose to click **Finish** before going through the wizard HDS starts with a new project and library, VHDL as the default language and all the available flows and tools. You can click **Finish** at any step to exit the wizard.

You can invoke the wizard at any time by choosing **HDS Setup Assistant** from the **Help** menu in the Design Manager window.

Using the HDS Setup Wizard

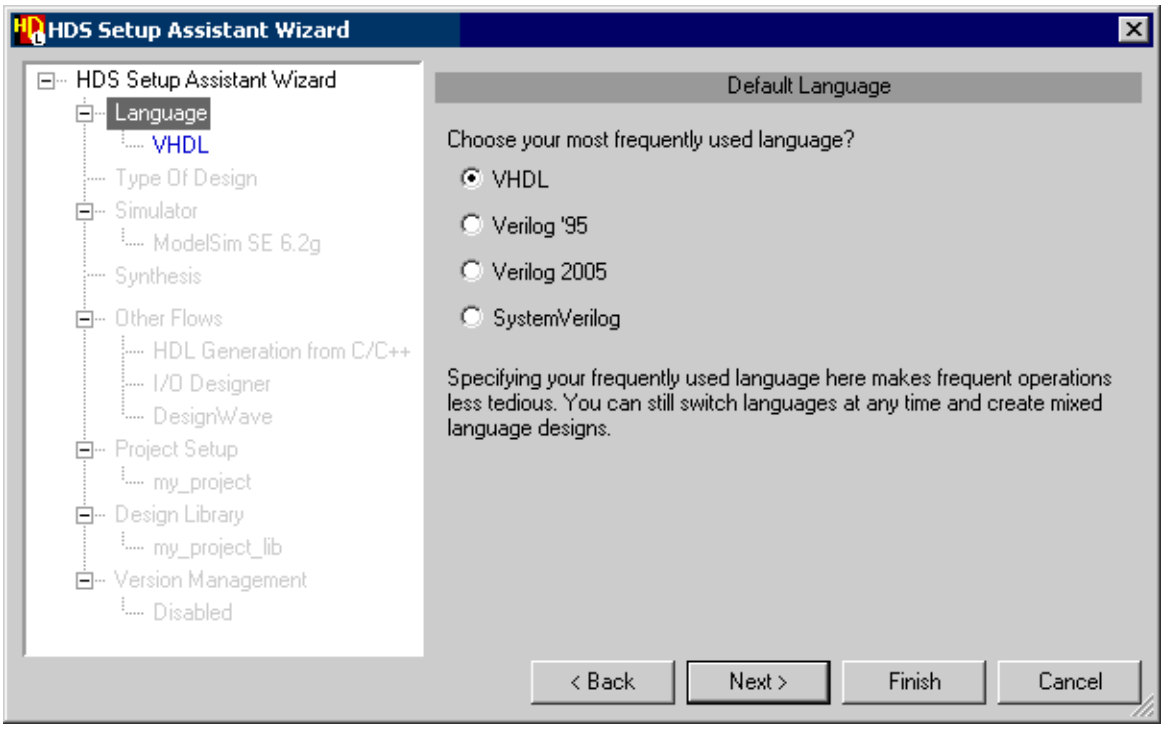


The left pane of the wizard displays a tree whose nodes represent the settings to be configured. These include Language, Type of Design, Simulator, Synthesis, Other Flows, Project Setup, Design Library and Version Management.

The first time the wizard is invoked you have to use the **Next** button to navigate through the left pane tree nodes. On moving to a new node the previous one is enabled.

The right pane of the wizard displays a page where you can configure the settings of the selected node.

Language Page

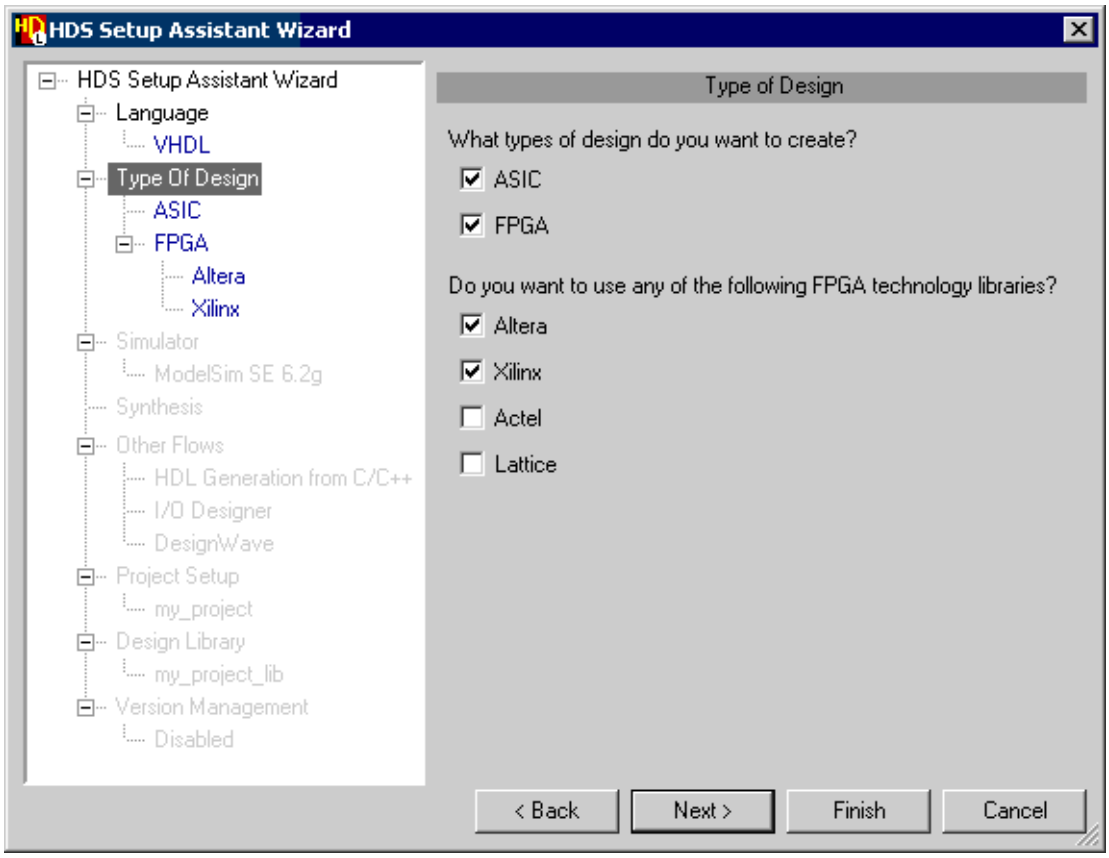


The language page enables you to specify the most frequently used language in creating new views. You can later change the default language used. Refer to “Main settings” in the *HDL Designer Series User Manual*. You can also specify a language for each new view created. Refer to “Design Content Creation Wizard” in the *HDL Designer Series User Manual*.

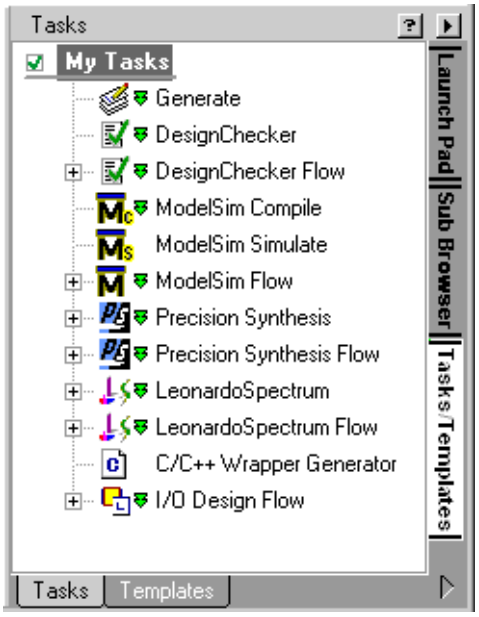
Design Page

You can optionally specify the type of designs you want to create as ASIC or FPGA. If you choose FPGA you can further specify the FPGA technology libraries as Altera, Xilinx, Actel or Lattice.

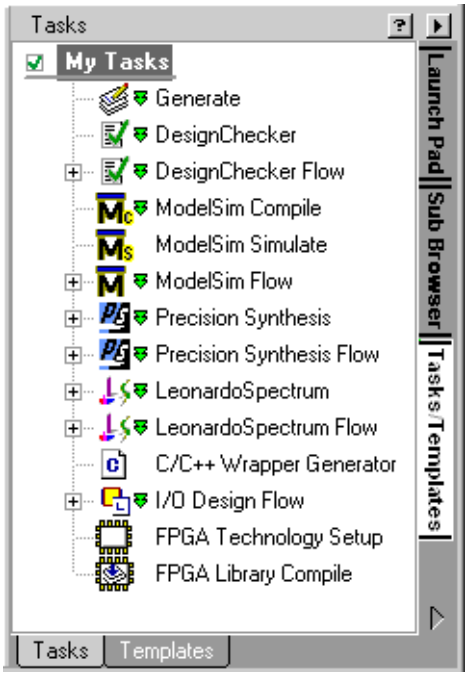
The tasks pane is automatically updated according to the design type you specify.



ASIC Default Task Pane

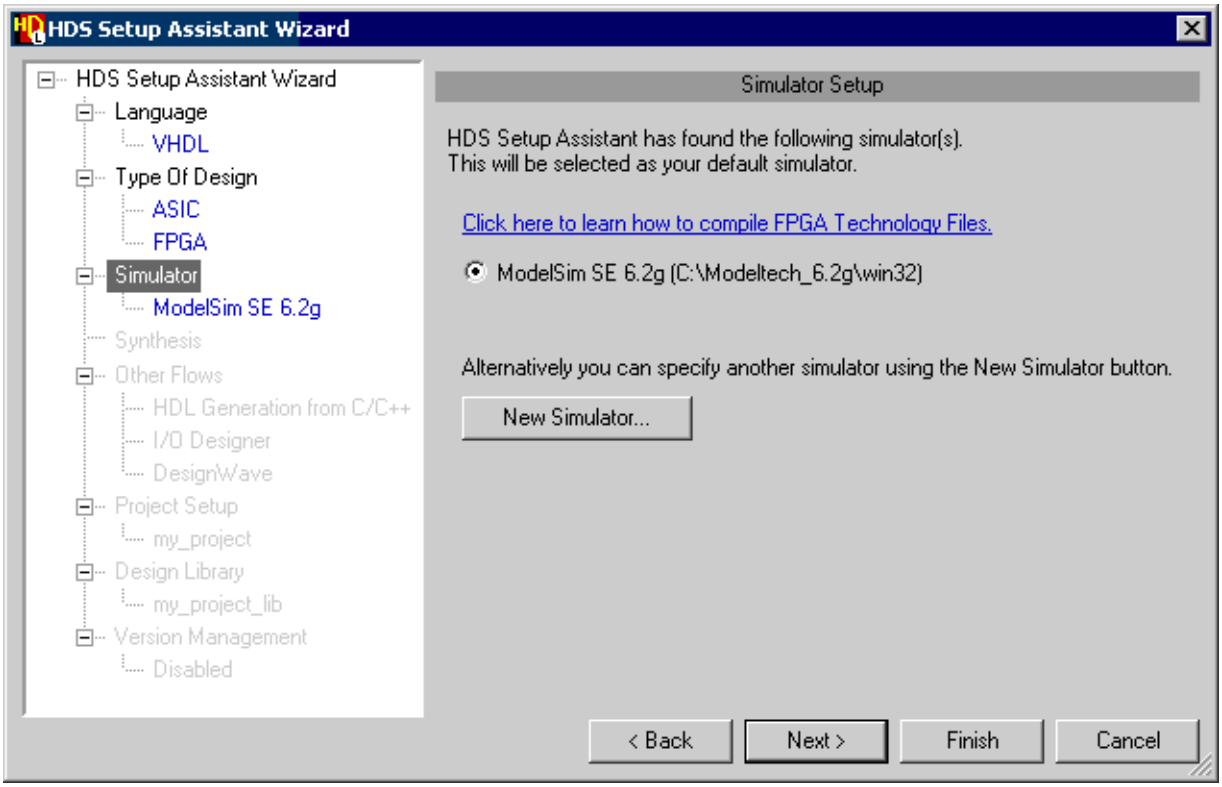


FPGA Default Task Pane

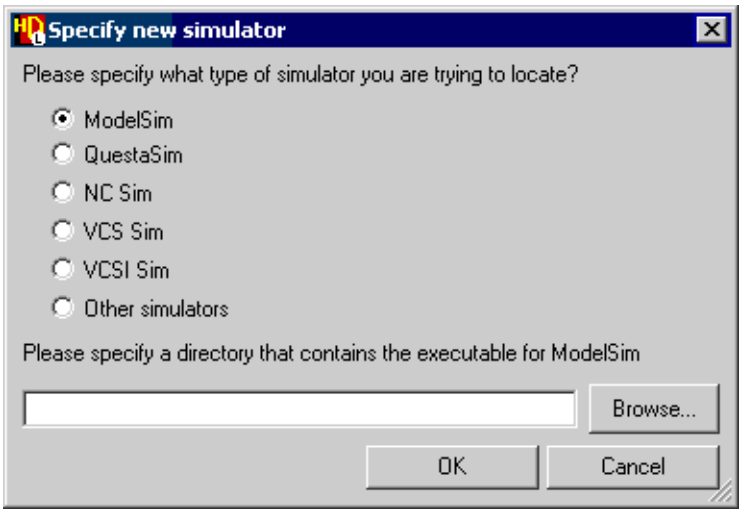


Simulator Page

HDS automatically detects the presence of any installed simulators. The simulator page displays a list of the detected simulators and sets the default.

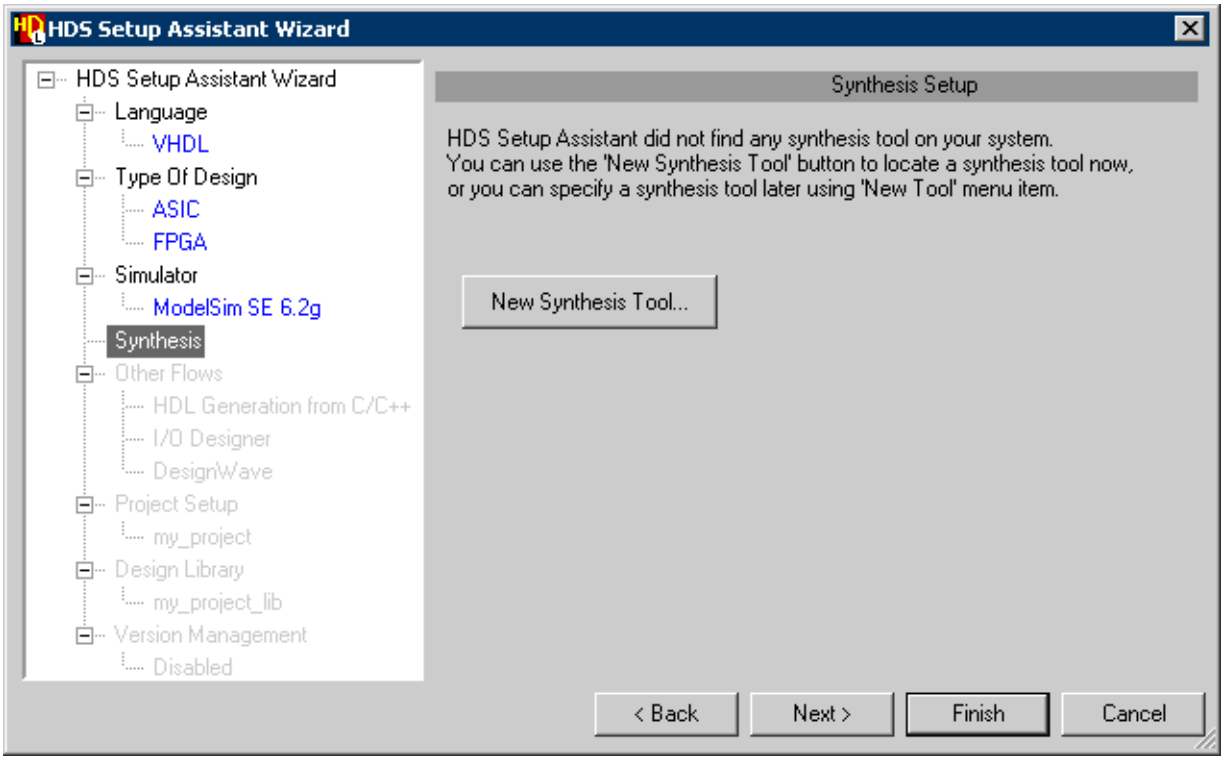


Alternatively you can specify a new simulator by clicking **New Simulator**.



Synthesis Page

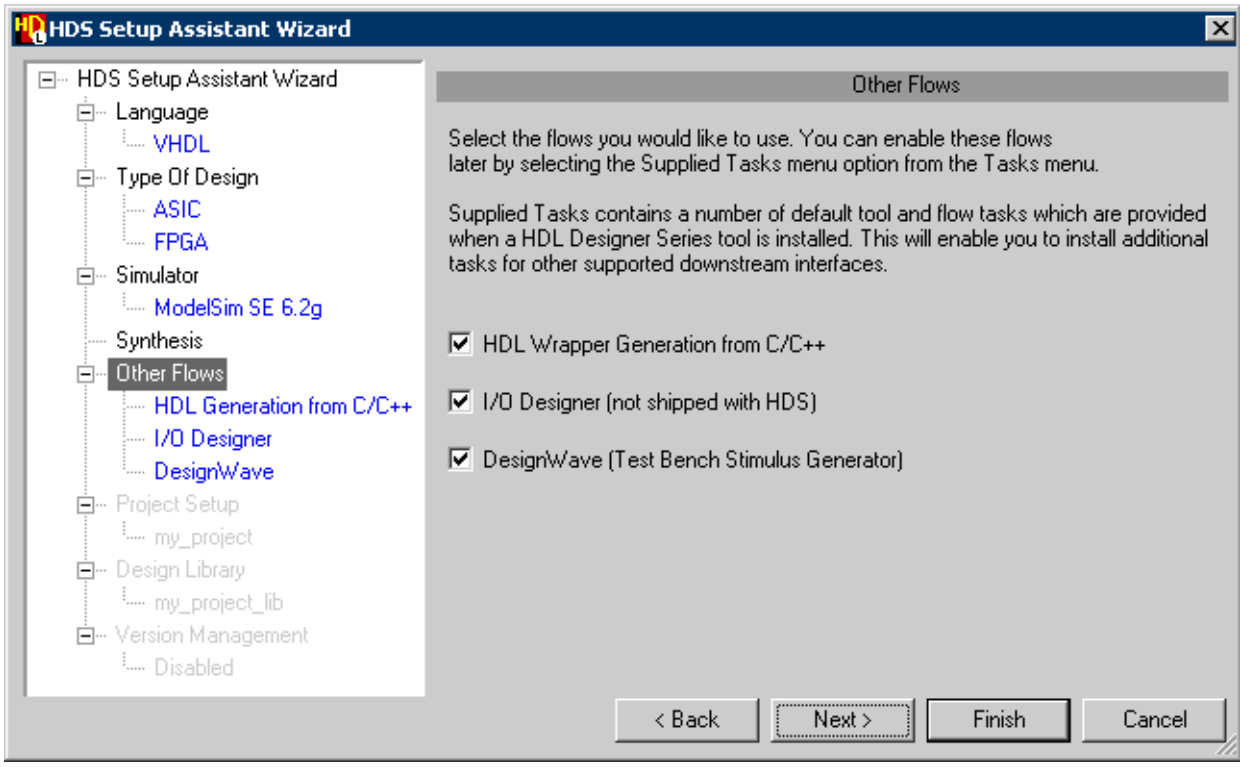
HDS automatically detects the presence of any installed synthesis tools. The synthesis page displays a list of the detected synthesis tools and sets the default.



Alternatively you can specify a new synthesis tool by clicking **New Synthesis Tool**.

Other Flows Page

The Other Flows page provides you with the option to select the flows you would like to use. You can add flows and tasks later.

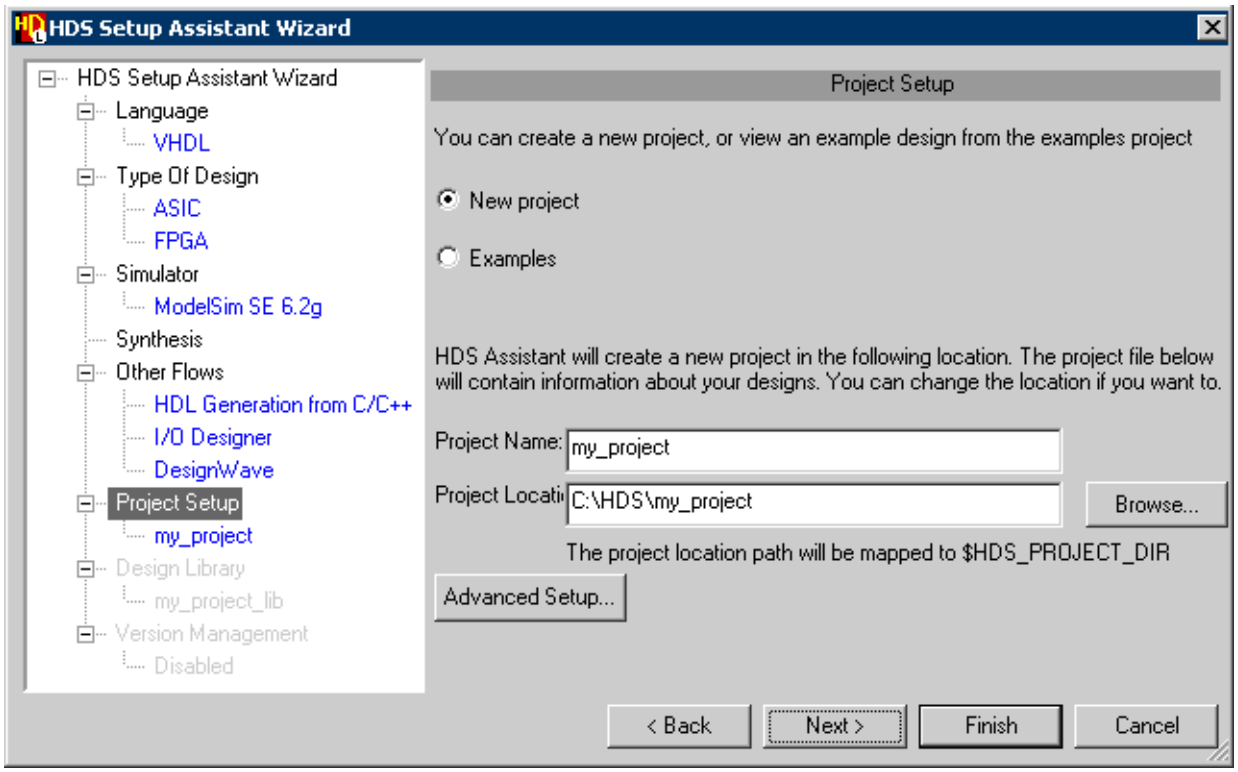


Project Setup Page

The Project Setup page gives you the option to start with a new project. You can alternatively choose to view one or all of the designs of the examples project.

To start with a new project:

1. Select New project.
2. Do one of the following:
   - Specify the Project name and location.
   - Click **Advanced Setup** to display the Project Setup Assistant.



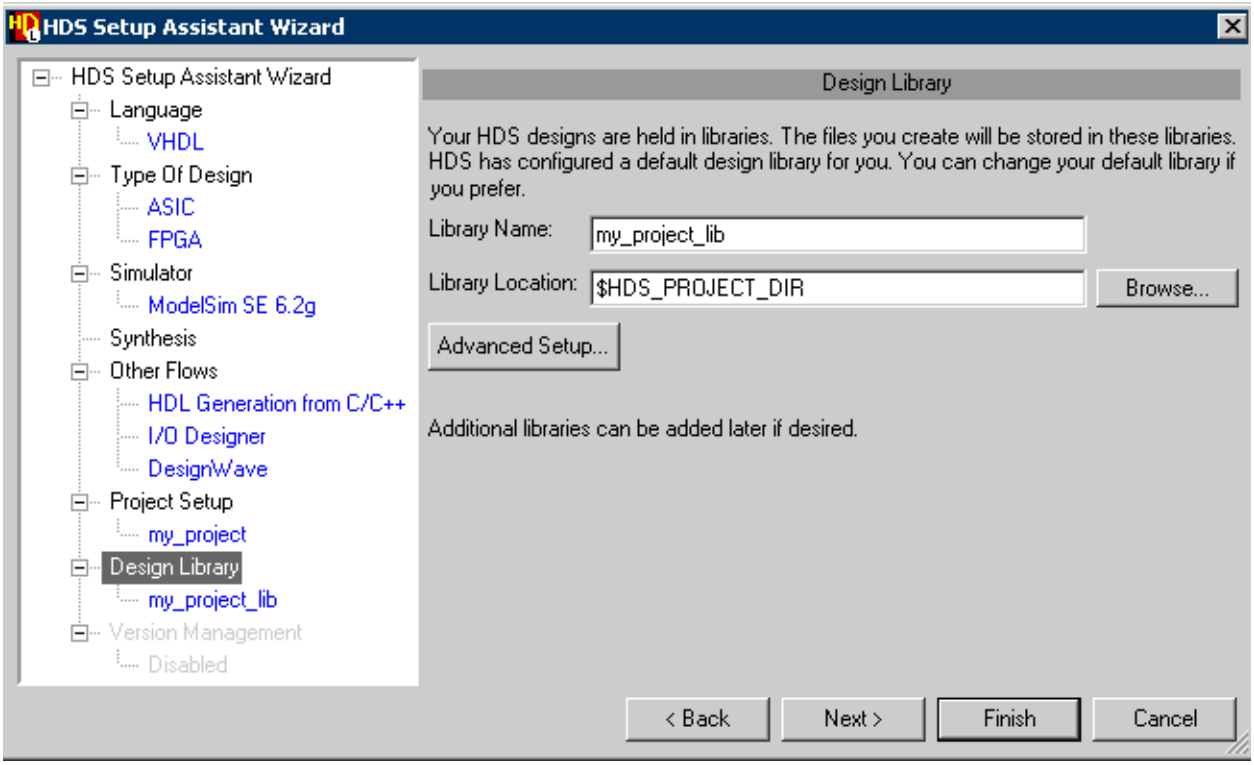
To start with the examples project:

1. Select examples to view a list of the design libraries included in the project.
2. Select a design library or the whole project to view.

Design Library Page

The Design Library page is active only if you had chosen to create a new project on the Project Setup page. It gives you the option to create a new library to save your design files.

To start with a new design library:



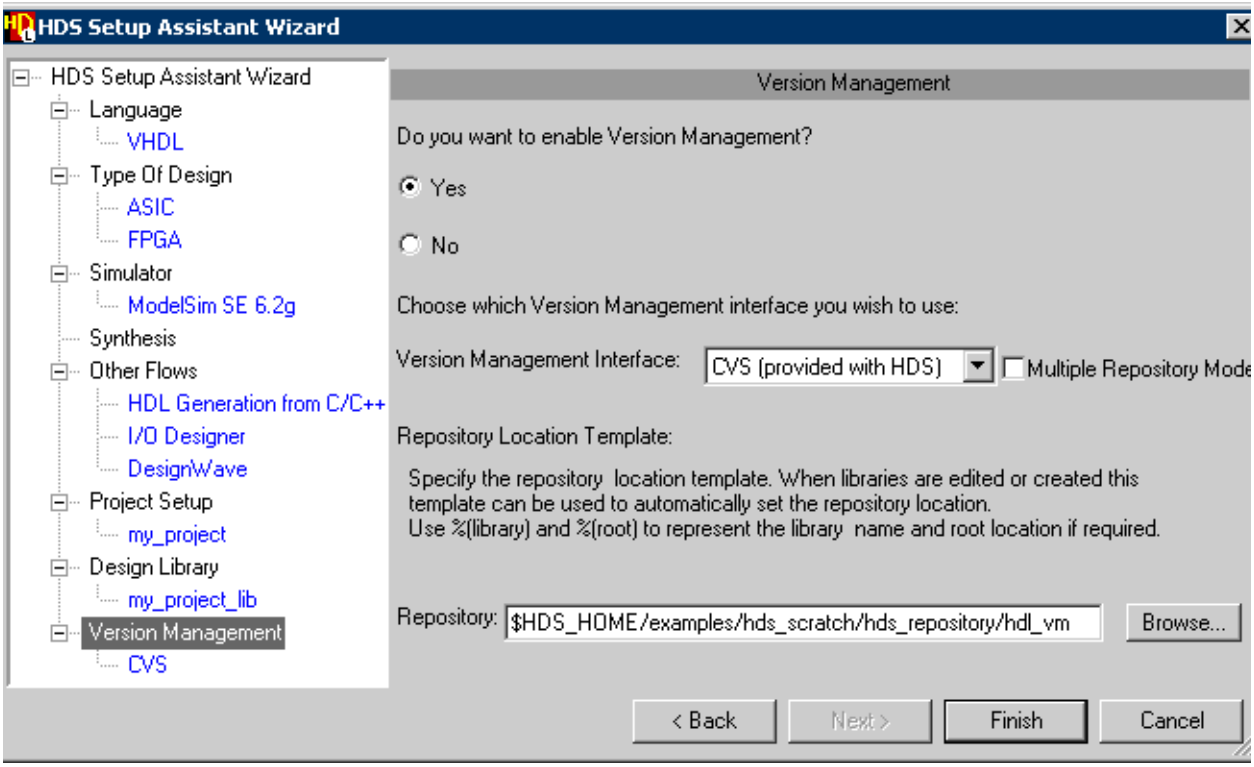
1. Select Yes.
2. Do one of the following:
   - Specify the Design library name and location. The default location is mapped to the project location specified on the Project setup page.
   - Click **Advanced Setup** to display the Design Library Setup Assistant.

Version Management Page

You can choose to enable version management. You can also specify the version management tool settings.

To enable version management:

1. Select Yes to display a dropdown list of the version management interfaces.
2. Select the version management tool.
3. Specify the version management settings if any.



The Default Project

When you invoke for the first time, the default project is defined by the following two project files:

My Project:*$HDS_HOME\examples\examples.hdp*
Shared Project:*$HDS_TEAM_HOME\shared.hdp*

Example Libraries

The following libraries are defined in the examples project:

- **SCRATCH_LIB —** An empty *Regular* library which is used as the default location for imported designs.
- **Ethernet —** This *Regular* library contains a HDL text design example which is part of the Ethernet IP core project and is reproduced under the terms of the GNU lesser general public license as published by the Free Software Foundation. For more information about the Ethernet IP project, see the web site:

  `http://www.opencores.org/projects/ethmac/`

The Ethernet design is defined by a mixture of VHDL and Verilog views and includes a test bench which can be used to simulate the design.

- **Sequencer_vhd** and **Sequencer_vlg —** These *Regular* libraries contain VHDL and Verilog versions of the Fibonacci sequencer design which is shown in many of illustrations used in this manual.

  The Sequencer design is also used for the procedures described in the *Design Exploration Tutorial*.

- **TIMER_Vhdl** and **TIMER_Vlog —** These *Regular* libraries contain completed VHDL and Verilog versions of a design which implements a timer design using block diagrams, a re-usable component defined by a HDL text view, a hierarchical state machine and truth table. The examples include a test bench controlled by a flow chart.

- **UART_TXT**, **UART, UART_V** and **UART_V2K—** These *Regular* libraries contain an example of a universal asynchronous receiver transmitter design with a test bench which can be used to verify the design if a HDL simulator is available on your system.

  The UART_TXT library contains a HDL text version of the design described by a mixture of VHDL and Verilog views and can be edited using any of the HDL Designer Series tools.

  The UART library contains a graphical version of the design described by VHDL views using block diagrams, IBD views, state machines, truth tables, flow charts and HDL text views.

  The UART_V library contains an alternative graphical version of the design described by Verilog.

  The UART_V2K library contains an alternative graphical version of the design described by Verilog 2005.

  The UART design is described in *"UART Example Design"* on page 33.

- **tinycache_sv_lib—** This library includes a SystemVerilog design.

Shared Libraries

The following libraries are defined in the default shared project:

- **exemplar —** A *Regular* library containing VHDL packages which support the LeonardoSpectrum synthesis tool.

- **hds_package_library —** A *Regular* library containing VHDL packages which support automatic type conversion within the HDL Designer Series tools. This library also contains packages which support the ModuleWare random value based waveform generator.

- **renoir_package_library —** This *Regular* library is provided for compatibility with older designs which used the type conversion packages. New designs should use the conversion functions in the *hds_package_library*.
- **moduleware —** This *Protected* library contains HDL function generators which can be instantiated as components in block diagram, IBD or HDL text views. The ModuleWare models are described in the *ModuleWare Reference Guide.*
- **std —** This *Protected* library contains STANDARD and TEXTIO standard VHDL packages.
- **ieee —** This *Protected* library contains the IEEE standard VHDL packages which are recognized by most downstream simulation tools.
- **std_developerskit —** This *Protected* library contains VHDL packages which support the development of VHDL models using the ModelSim simulation tools.
- **synopsys —** This *Protected* library contains VHDL packages to support the Synopsys Design Compiler synthesis tool.
- **verilog —** This *Protected* library contains definitions for the standard Verilog types.

The *hds_package_library* (or *renoir_package_library*) and *exemplar* package libraries must be compiled to make them available for use.

You should add downstream mapping for these libraries to a location where you have write permission. After compiling these libraries, they should be changed to *Protected* libraries to avoid accidental regeneration or recompilation.

The contents of the standard VHDL packages are described in the “VHDL Standard Libraries” section of the *HDL Designer Series User Manual*.

Using the Example Designs

The example designs can be opened as read-only reference examples. Windows users typically have write access to these designs. However, it is recommended that you copy the design to a suitable directory for user data.

The directories for source data, generated HDL and downstream data can be anywhere on your file system. Typically, you may use separate subdirectories within the same tree. For example, the UART libraries are mapped to *hds*, *hdl* and *work* directories beneath a common *uart* (or *uart_v*) directory.

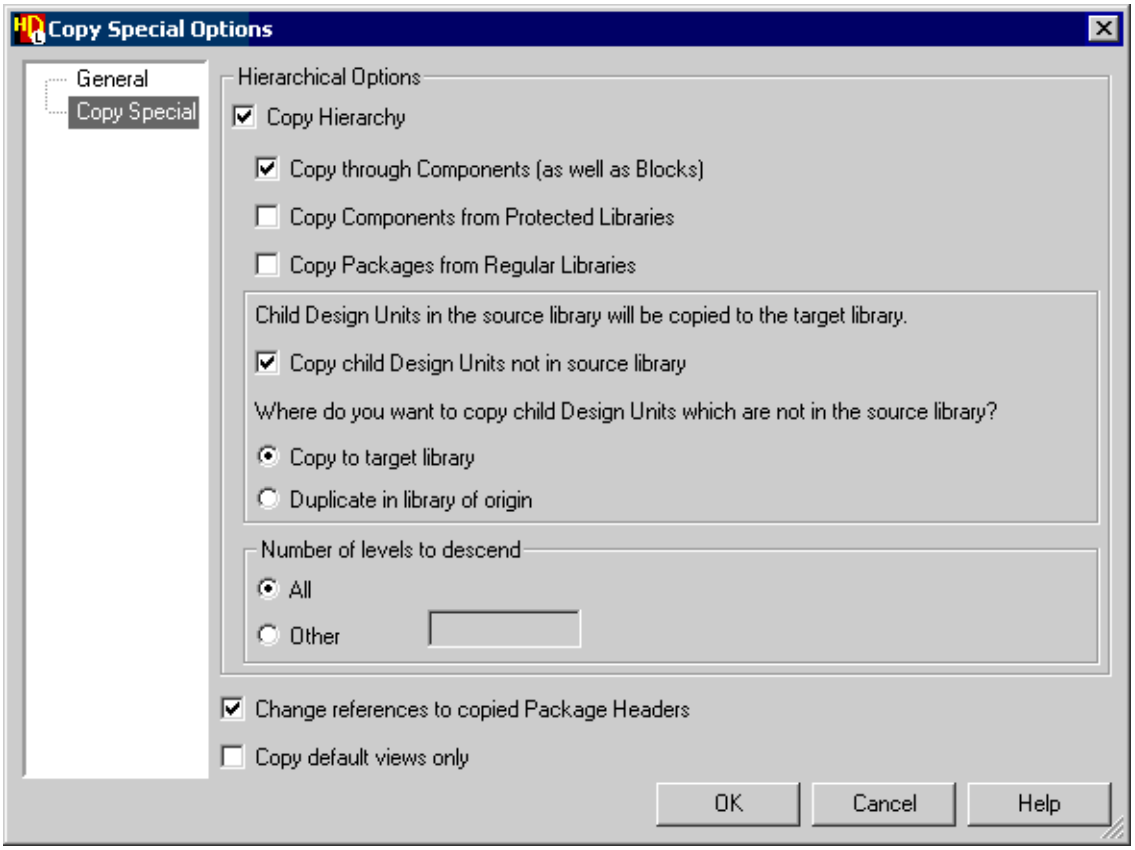
If you want to use the GNU Concurrent Versions System (CVS), the source data must be in a directory which exactly matches the name of the library. Refer to “Creating a Library Mapping” in the *HDL Designer Series User Manual* for more information.

Use the following procedure to make a copy of the example library:

1. Set library mapping (including HDL HDS source, and downstream directories to which you have write permission) for a new empty library.
2. Select the new library and the library you want to copy in the project manager. Choose **Explore Library** from the **File** or popup menu to open both libraries in a new design explorer window.
3. Select the top level design unit in the example library and drag it over the new library name with the Right mouse button.
4. Choose **Copy Special Here** from the popup menu which is displayed when you release the mouse button to display the Copy Special Options dialog box.
5. Select **Copy Through Components**, **Copy to target library** and **All** levels in the dialog box.
6. Confirm the dialog box.

A complete logical copy of the origin library is made in the target library. All references in the new library to objects in the original library are updated to reference the new library.

Note that, HDL filenames are derived from the logical names of the HDL text views. (For example, if you copy the *TIMER_Vlog* library, the *BCDCounter* view is copied to a new file named *BCDCounter.v*.)



You can also copy a library by selecting the library name in the design explorer and choosing **Copy Contents** from the popup menu and then using the **Paste** command to make a physical copy in the new library.

When you use these commands, all the files in the origin library are copied. (For example, if you copy the *TIMER_Vlog* library, the *BCDCounter* view is copied to a new file named *Timer_BCDCounter.v*, preserving the original file name used in the origin library.)

The new library can be browsed, edited, generated, compiled, simulated, animated or synthesized without any impact on the original examples.

If you want to animate any flow charts and state diagrams in an example design, you should set **Instrument HDL for animation** in the properties for the state machine and flow chart and then regenerate the HDL through components.

Appendix A
UART Example Design

The Universal Asynchronous Receiver Transmitter (UART) design is provided as a mixed VHDL and Verilog HDL text design and as separate graphical VHDL and Verilog versions to illustrate the key design creation facilities provided by the HDL Designer Series products.

Overview

The design is a UART which provides serial communications between a CPU (such as an ARM processor) and a Serial Device. The full specification for the device can be found at the end of this document.

- Different baud rates can be set for the transmit/receive clock divider. This can be done by writing the most significant and least significant divide values into the **divmsb** and **divlsb** registers.
- Data is transmitted by writing the 8 bit value into the **xmitdt** register. The interrupt line (**int**) goes high when the transmit cycle is completed. The data is placed on the serial out line (**sout**) with the appropriate start and stop bits.
- Serial data is received into the **recvdt** register. The interrupt line (**int**) goes high when a correctly constructed word has been received.
- Any internal register can also be read by the CPU.
- A Status Register contains flags to indicate when transmission or receiving is in progress or completed.
- The status register and hence the interrupt can be cleared by reading register address 7.

Two graphical versions of the design are provided in the libraries *UART* (VHDL) and *UART_V* (Verilog). Both of these graphical designs are partitioned as follows:

```
UART
uart_tb (struct - block diagram)
   tester (flow - flow chart)
   uart_top (struct - block diagram)
      clock_divider (flow - flow chart)
      cpu_interface (intconx - IBD; struct - block diagram)
         data_out_mux (embedded HDL text)
         control_operation (fsm - hierarchical state diagram)
      serial_interface (struct - block diagram)
         convert (embedded flow chart)
         zeros (ModuleWare)
         status_registers (spec - hand-written HDL)
         ser_out_mux (ModuleWare)
```

```
      xmit_rcv_control (fsm - concurrent state diagram)
   address_decode (tt - truth table)
```

Note

The CPU interface is described by an IBD view but an alternative block diagram view is also provided.

A third UART_TXT library describes the UART using a mixture of VHDL and Verilog HDL text views without any graphical views:

```
UART_TXT
uart_tb (rtl - Verilog text)
   tester (rtl - Verilog text)
   uart_top (rtl - VHDL text)
      clock_divider (rtl - Verilog view)
      cpu_interface (rtl - VHDL text)
         control_operation (rtl - VHDL text)
      serial_interface (rtl - VHDL text)
         status_registers (rtl - VHDL text))
         xmit_rcv_control (rtl - VHDL text)
      address_decode (rtl - VHDL text)
```

Design Description (uart_top)

The starting point for the design is the top-level block diagram. This diagram describes the top-level functional blocks of the device. A component symbol can be automatically created from the block diagram. Alternatively, the symbol can be created first, from the input/output specification and the top-level block diagram created as an underlying description.

The CPU has the ability to reset the UART and to read to and write from the registers in the UART. The Serial Device can either be receiving data from the UART or transmitting data to the UART.

UART Interface

The UART interface is designed for use with an ARM processor and consists of the following signals:

- **data_in[7:0] —** This is the 8-bit input data bus which carries the data which the CPU writes to the UART registers.
- **data_out[7:0] —** This is the output data bus which carries the data from the selected UART register.
- **addr[2:0] —** This is the address bus which is connected to the CPU. This signal indicates which register is being written or read by the CPU.
- **sin —** This is the serial input signal from the external serial device. When serial data is being read, the register *rcvdt* is loaded with individual bits from this signal.

- **sout —** This is the serial output signal to the external serial device. The contents of *xmitdt* register is output one bit at a time.
- **int —** This signal indicates that serial data has been transmitted or received successfully and requests an interrupt from the CPU.
- **cs —** This Chip Select signal is asserted low to enable transmit and receive cycles.
- **nrw —** notRead/Write. ’0’ indicates a Read operation, ’1’ indicates Write.
- **clk —** The main system clock. 50% duty cycle. Typically 100ns clock period.
- **rst —** Active low asynchronous reset.

UART Structure

The four top-level blocks are:

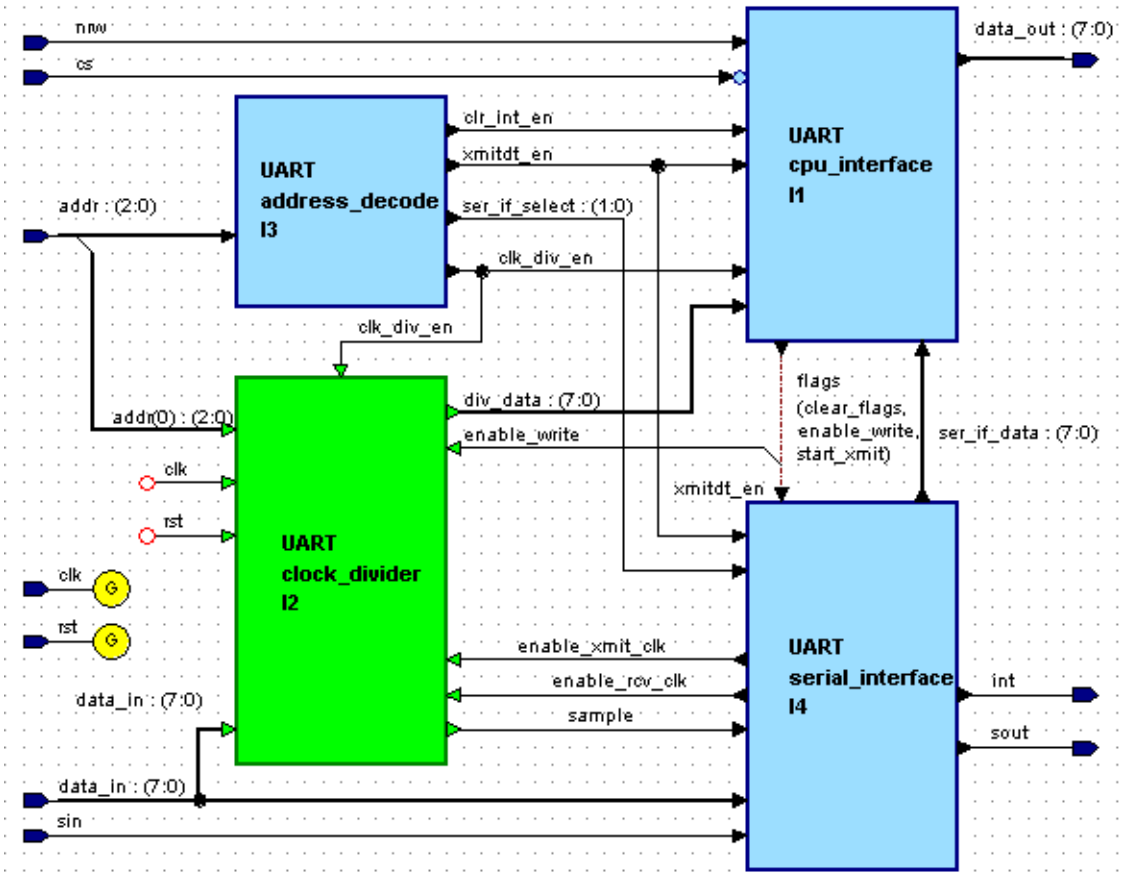
- **address_decode —** Uses the lowest 3 bits of the CPU address bus to determine which register is being addressed.
- **clock_divider —** Provides a sampling clock for transmitting and receiving serial data. The baud rate is determined by the two-byte divisor value (*divlsb*, *divmsb*) used to divide down the main system clock.
- **cpu_interface —** This block controls whether the UART is transmitting, receiving or clearing the status flags (and interrupt). It also provides CPU access to the internal UART register information.
- **serial_interface —** Performs the actual transmission and receiving of serial data. It also stores the status flags and generates the interrupt. This block also provides the transmit/receive register information to the *cpu_interface*.

Address Decode

The *address_decode* block is defined as a truth table. It decodes the last 3 bits of the address bus (**addr**) to provide a set of enable signals indicating which register is being addressed:

- **clk_div_en —** This is set if either **divlsb**(0) or **divmsb**(1) of the clock divider registers is being addressed.
- **xmitdt_en —** Indicates transmit register (**xmitdt**) is being addressed.
- **ser_if_select —** Contains the last two bits of the address bus which are used to select the register to output onto the **ser_if_data** bus.

- **clr_int_en —** A "pseudo register" which, when read, causes the status flags and interrupt flag to be cleared.



Clock Divider

The *clock_divider* is described as a flow chart. The divider can be asynchronously reset otherwise the divider either loads in the 2-byte divider value or counts clock edges. The resulting output signal **'sample'** is a 50% duty cycle divided clock. This is used as the clock for transmission and receiving operations.

CPU Interface

The *cpu_interface* is described by an IBD view which performs two operations:

- **control_operation —** determines which mode of operation the UART is in (transmit, receive, clearing).
- **data_out_mux —** places the clock divider value (**div_data**) or serial interface register information (**ser_if_data**) onto the CPU **data_out** bus depending on the value of **clk_div_en**.

Control Operation

The register operations of the UART are controlled by the signals **nrw** and the chip select flow, **cs**. The *control_operation* component is described as a hierarchical state machine which consists of a top-level state **waiting** (also the reset state) and two hierarchical states for transmit (**TX**) and receive (**RX**).

The following states can be implied from the UART specification:

- **waiting —** No register read or write operations have been requested by the CPU.
- **TX/writing_to_reg —** Output **enable_write** is set. Data is being taken from the **data_out** bus and is being written to the register indicated by the address bus (**addr**).
- **TX/xmitting —** Output **start_xmit** is set. The UART is transmitting data to the serial output flow (**sout**). This occurs after the **xmitdt** register (4) has been written.
- **RX/reading_from_reg —** Data is being taken from the register indicated by the address bus (**addr**) and is being written to the **data_out** bus.
- **RX/clearing_flags —** Output **clear_flags** is set. The UART is clearing the status register (**status**) and resetting the interrupt flag (**int**). This occurs after register 7 has been read.

The outputs from the *control_operation* component are:

- **enable_write —** Indicates that a register should be written; data should be taken from the input data bus (**data_in**).
- **start_xmit —** Indicates that serial data transmission should commence.
- **clear_flags —** Indicates that the internal flags (associated with transmitting and receiving) should be cleared.

Data Out Mux

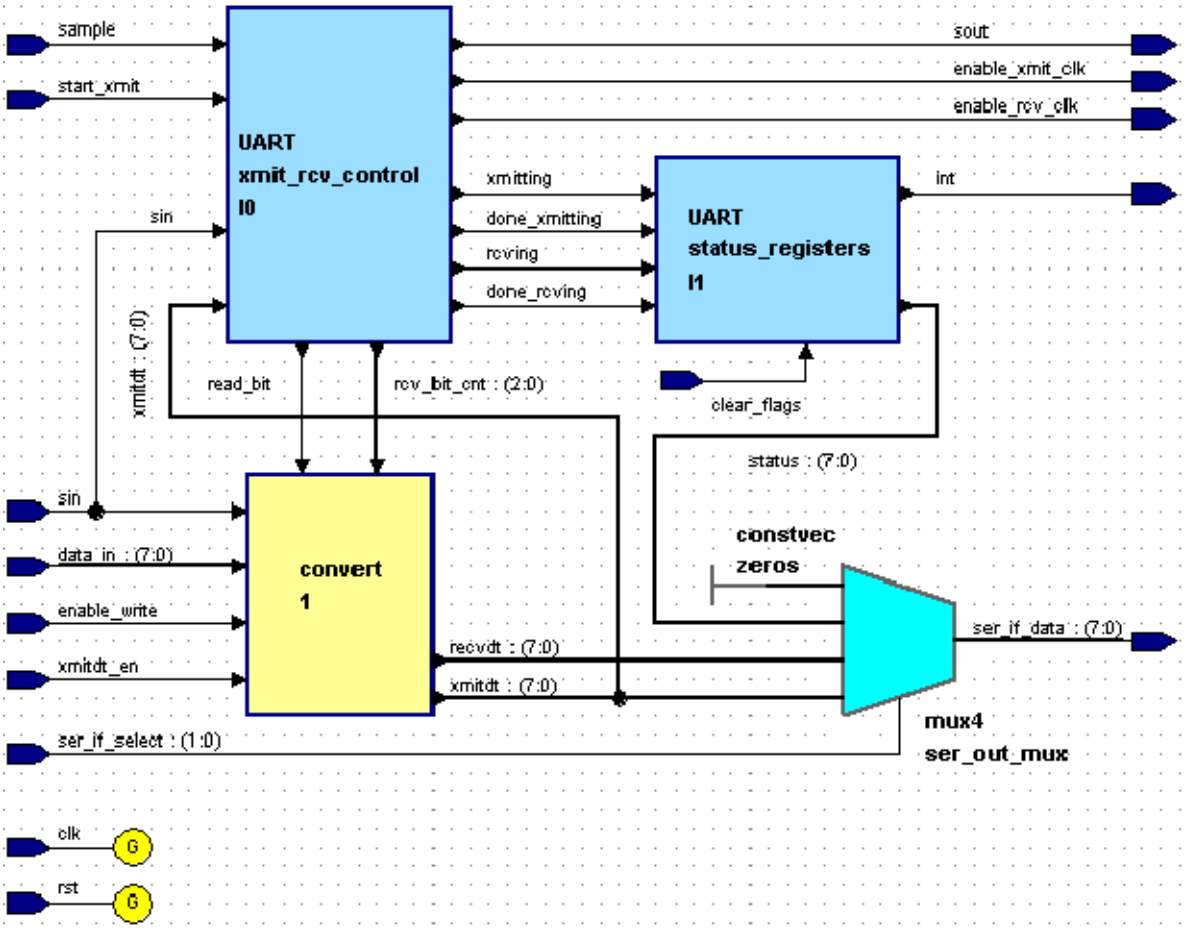
- The *data_out_mux* is described by an embedded HDL text block. The output placed on the CPU **data_out** bus is determined by the **clk_div_en** signal. If **clk_div_en** is ’1’, the clock divider value (**div_data**) from the *clock_divider* block is output, otherwise the serial interface information from the *serial_interface* block is output.

Serial Interface

The *serial_interface* block consists of four main functions:

- **xmit_rcv_control —** Controls the transmitting and receiving of serial data to/from the external serial device.
- **status_registers —** Stores the transmit and receive status flags, composes the **status** byte and produces the interrupt (**int**).

- **convert —** Loads the transmit data from **data_out** into the **xmitdt** register and composes the receive register (**recvdt**) from the incoming serial data stream (**sin**).
- **ser_out_mux —** places the contents of the transmit data register (**xmitdt**) or the receive register (**recvdt**) or the status byte (**status**) onto the serial interface data bus (**ser_if_data**) depending on the value of **ser_if_select**.



The following internal signals provide communication between the blocks:

- **xmitting —** Indicates that data is being transmitted to the serial device and that the appropriate status bit of the status register should be set.
- **done_xmitting —** Indicates that transmission to the serial device has just finished and that the appropriate status bit of the status register should be set.
- **rcving —** Indicates that data is being received from the serial device and that the appropriate status bit of the status register should be set.
- **done_rcving —** Indicates that data has been received from the serial device and that the appropriate status bit of the status register should be set.

- **read_bit —** Indicates that one bit of data should be loaded into part of the receiving register (**recvdt**).
- **rcv_bit_cnt —** Indicates the bit position into which the serial data should be read.
- **xmitdt —** Contains the data which will be transmitted to the serial device.

Xmit Rcv Control

The UART specification describes, step-by-step, how serial data is transmitted and received. These operations are performed by two concurrent state machines, one for the transmitting of data (*Xmit*), and one for the receiving of data (*Rcv*). Although both machines run with the system clock (**clk**) the transmit and receive baud rate is determined by the divided clock "**sample**".

- ***Transmit (Xmit)***
  After register 4 (**xmitdt**) is written, control_operation sets **start_xmit** which causes serial transmission to commence. After sending an initial ’0’ start bit, the transmit clk (**sample**) is enabled and the xmitting flag set.

  The contents of the xmitdt register is placed on the serial line (**sout**) one bit at a time on the rising edge of **sample**. Once all 8 bits have been transmitted, a ’1’ stop bit is sent, the **done_xmitting** is flag set and the sample clock is disabled.
- ***Receive (Rcv)***
  Serial data is received when the serial input flow **sin** goes low (and remains low for a specified amount of time). If lock is achieved, the receive clock (**sample**) is enabled and the receiving flag set.

  The signal **read_bit** is set/reset for the following 8 rising/falling edges of **sample**. The stop bit is skipped, the **done_rcving** flag is set and the sample clock is disabled.

Status Registers

The *status_registers* block is described directly in HDL. This block registers the transmit and receive status flags (**xmitting**, **done_xmitting**, **rcving**, **done_rcving**) and to compose the 8-bit status byte from these flags. Once the done flags are set, they remain at ’1’ until cleared. The interrupt signal (**int**) is set if the **done_xmitting** or **done_rcving** flags are set. The status flag registers (and hence the status byte and interrupt) are cleared by either the **clear_flags** signal from *control_operation* or by the system reset (**rst**).

Convert

The *convert* embedded block is described as a flow chart. This block loads and stores the **xmitdt** and **recvdt** registers. Both registers are cleared by the system reset (**rst**) asynchronously. On the system clock edge (**clk**), if **xmitdt_en** and **enable_write** are both set, the transmit register (**xmitdt**) is loaded with the value from the CPU on the **data_in** bus. Otherwise, if

read_bit is set, then the current serial input value (**sin**) is loaded into the appropriate bit of the receive register (**recvdt**).

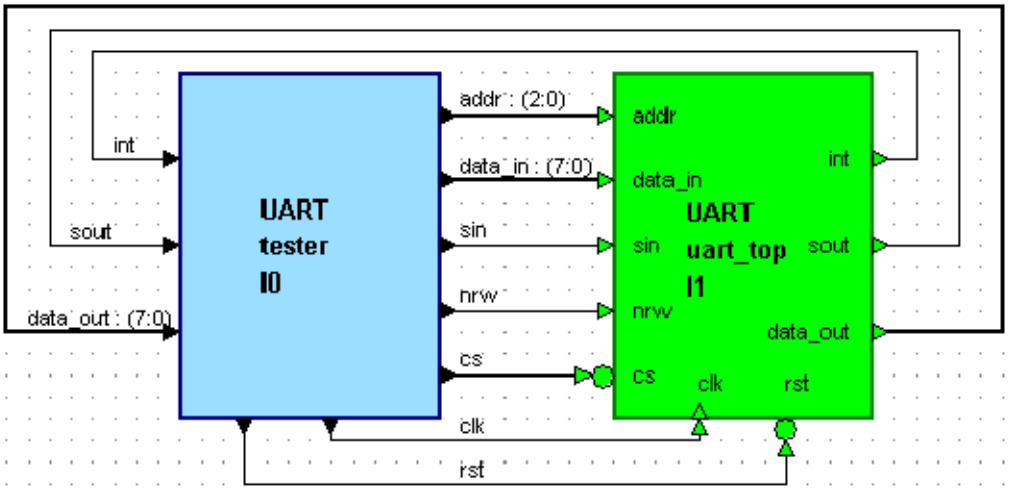
Ser Out Mux

The serial output multiplexer block *ser_out_mux* consists of an 8-bit constant (*constvec*) providing an all zero output vector and a 4-input, 8-bit multiplexer (*mux4*) implemented by ModuleWare components. The output **ser_if_data** is assigned the value of the **xmitdt**, **recvdt** or **status** registers depending on the value of the **ser_if_select** signal. **ser_if_data** is connected to the *data_out_mux* in the *cpu_interface* for output to the CPU **data_out** bus.

Test Bench (uart_tb)

The design library includes a test bench component, *uart_tb*. This is a block diagram containing an instance of the uart itself (*uart_top*) with all inputs and outputs connected to a tester block (*tester*). The *tester* block is described using a flow chart, which is well-suited to the procedural/sequential nature of test functions. The tester performs the following test sequence:

- Initialize inputs and perform system reset
- Test serial data transmission:
  - Write "06" into clock divider LSB
  - Write "00" into clock divider MSB
  - Write "5A" into the transmit register (**xmitdt**)
  - Check interrupt (**int**) is asserted after serial transmission
  - Clear interrupt (**int**) by reading register 7



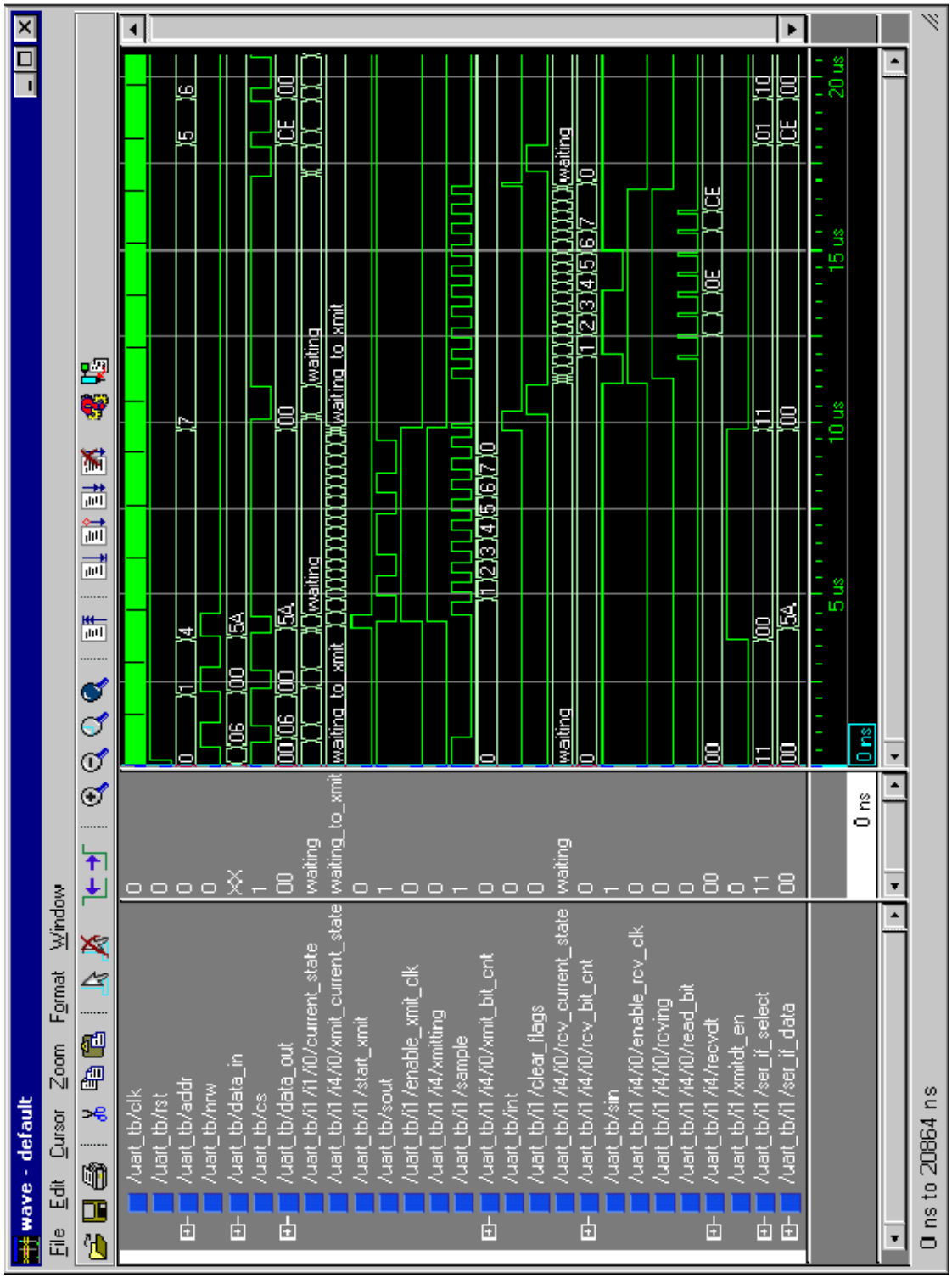
- Test serial data receive:

  - Place start bit (’0’) onto serial input line (**sin**)
  - Place serial data "CE" (11001110) onto serial input line (**sin**) starting with the least significant bit
  - Place stop bit (’1’) onto serial input line (**sin**)
  - Clear interrupt (**int**) by reading register 7
  - Read receive register (**rcvdt**)
  - Check value in receive register is same as the serial data sent to the UART ("CE")
- Test status:
  - Read status register (**status**)
  - Check all bits are zero

The *tester* flow chart description also contains a clock generator in the concurrent statements section and procedures in the process declaration section to perform the uart read and write functions. The declarations include constants for the system clock period (100ns) and the test transmit and receive data.

Simulation Results

The simulation results should be similar to those shown overleaf.


wave - default
File Edit Cursor Zoom Format Window
/uart_tb/clk
/uart_tb/rst
/uart_tb/addr
/uart_tb/nrw
/uart_tb/data_in
/uart_tb/cs
/uart_tb/data_out
/uart_tb/i1/i0/current_state
/uart_tb/i1/i4/i0/xmit_current_state
/uart_tb/i1/start_xmit
/uart_tb/sout
/uart_tb/i1/enable_xmit_clk
/uart_tb/i1/i4/xmitting
/uart_tb/i1/sample
/uart_tb/i1/i4/i0/xmit_bit_cnt
/uart_tb/int
/uart_tb/i1/clear_flags
/uart_tb/i1/i4/i0/rcv_current_state
/uart_tb/i1/i4/i0/rcv_bit_cnt
/uart_tb/sin
/uart_tb/i1/i4/i0/enable_rcv_clk
/uart_tb/i1/i4/i0/rcving
/uart_tb/i1/i4/i0/read_bit
/uart_tb/i1/i4/recvdt
/uart_tb/i1/i4/xmitdt_en
/uart_tb/i1/ser_if_select
/uart_tb/i1/ser_if_data
waiting
waiting_to_xmit
0 ns
5 us
10 us
15 us
20 us
0 ns to 20864 ns

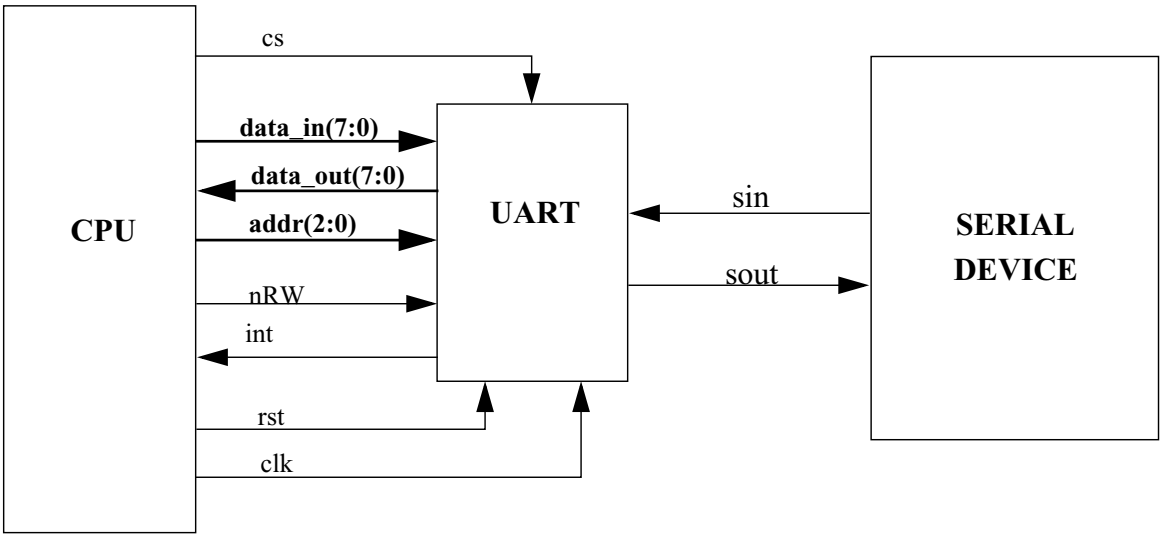
UART Specification

UART Registers

The UART contains 6 registers, each 8 bits wide:

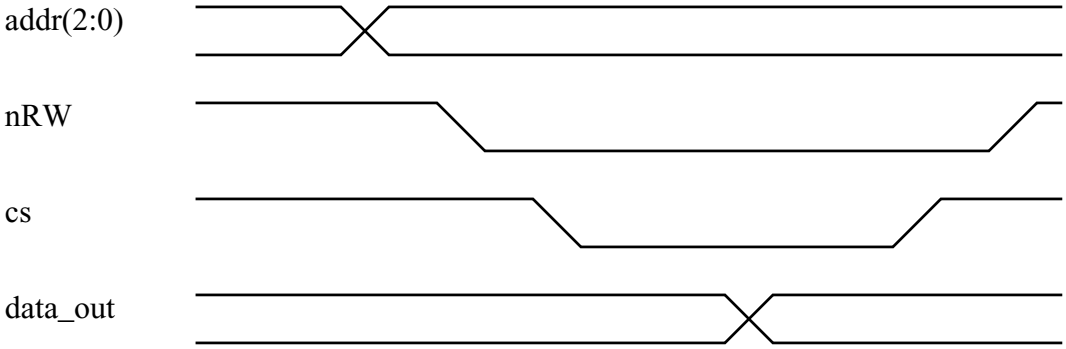
```
0  DIVLSB   Contains Least Significant bits of Clock Divider
1  DIVMSB   Contains Most Significant bits of Clock Divider
2  Unused
3  Unused
4  XMITDT   Contains data to be transmitted
5  RECVDT   Contains received data
6  STATUS   Contains UART Status
            bit 0    Indicates transmitting in progress
            bit 1    Indicates receiving is in progress
            bit 2    Indicates transmission is done
            bit 3    Indicates receiving is done
7  CLRINT   When read from, clears the interrupt flag as well
            as receive and transmit done flags
```

UART Application



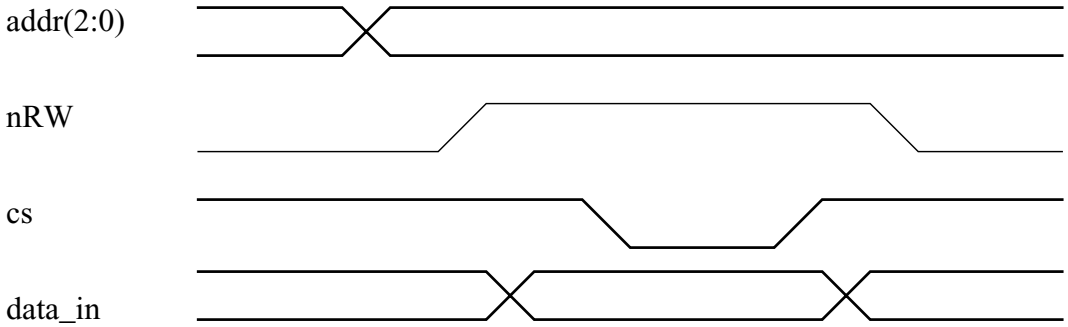
- Reset UART
- Read UART registers
- Write UART registers
- Transmit data
- Receive data

Reading from a UART Register



- If **cs** is low and **nRW** is low, put the content of the UART register addressed by **addr** onto the **data_out** bus.
- If the address was 7 (CLRINT) then clear interrupt flag and transmit and receive done bits in status register.

Writing to a UART Register



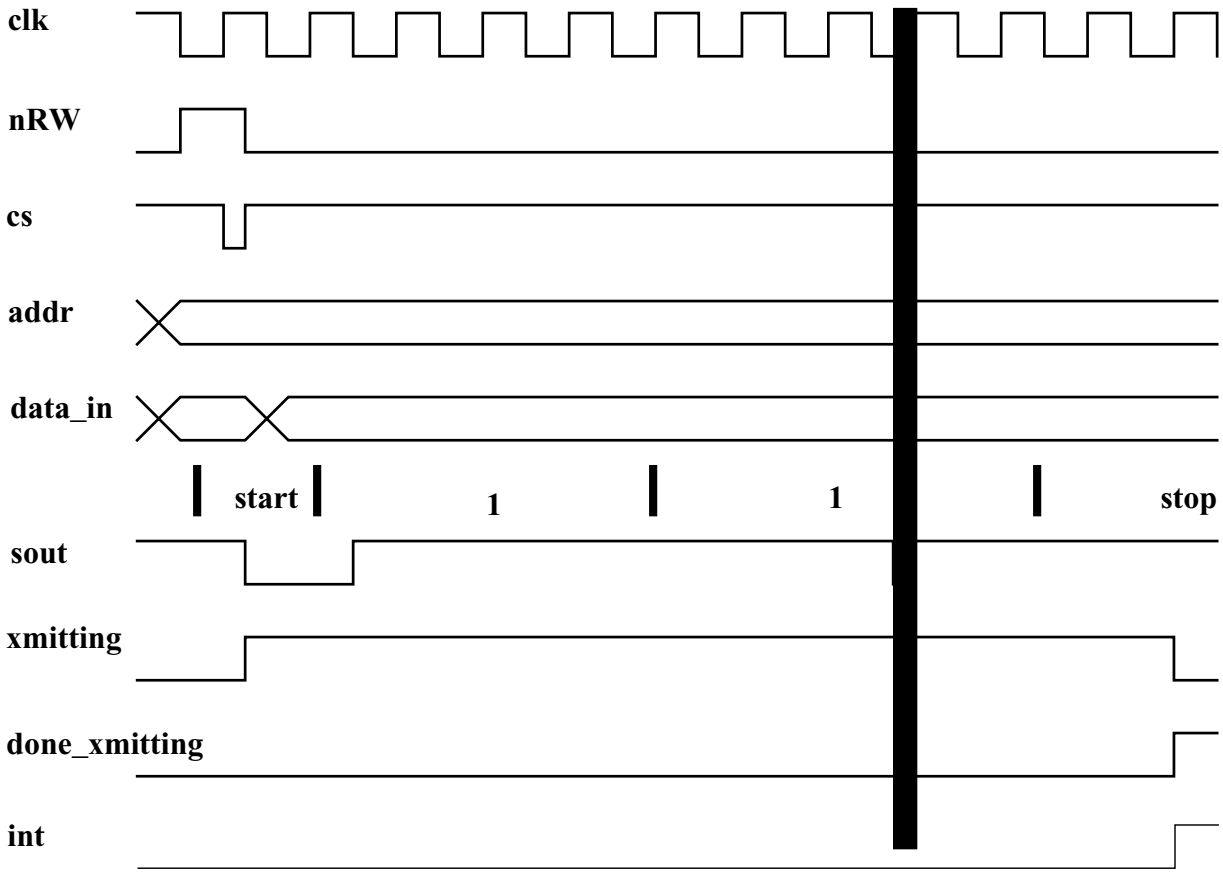
- If **cs** is low and **nRW** is high, save **data_in** in the UART register addressed by **addr**.
- If the address was 4 (XMITDT) then start transmitting content of the xmitdt register to the serial device.

Transmitting Data

If the last operation from the CPU was write to register number 4 (**xmitdt**) then start transmitting content of **xmitdt** register, one bit at a time.

- Set transmitting bit in the status register to one (bit 0 of status register).
- Enable the transmit clock.
- Send start bit (a zero bit half of the duration of the transmit clock).
- Send content of register number 4 one bit at a time starting with least significant bit first.

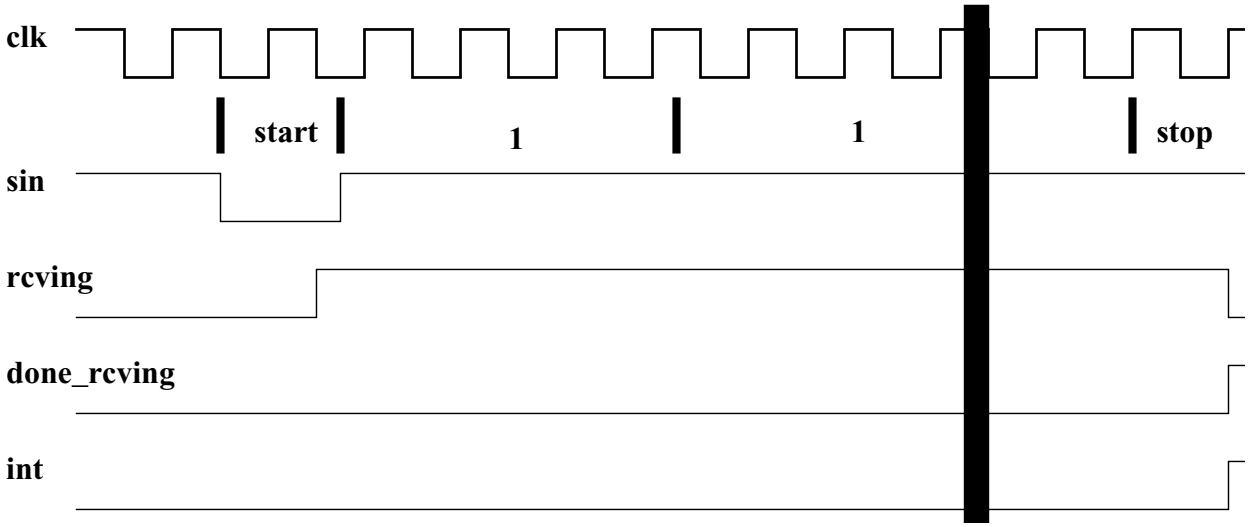
- Send stop bit (a one bit).
- Clear transmitting bit in the status register.
- Set done transmitting bit in the status register to one (bit 2 of status register).
- Set interrupt flag to one.



Receiving Data

- Wait for falling edge of **sin**.
- Wait for half of receive clock (**sample**) cycle.
- If **sin** is still low (start bit), start receiving data, otherwise abort operation and wait for another falling edge of **sin**.
- Set receiving bit in the status register to one (bit 1 of status register).
- Enable the receive clock.
- Receive data, one bit at a time starting with least significant bit (including stop bit).

- Save received data in register number 5 (**recvdt**), strip off the stop bit.
- Clear receiving bit in the status register.
- Set done receiving bit in the status register to one (bit 3 of status register).
- Set interrupt flag to one.



Appendix B
Environment Variables

Environment variables are used to locate the license server. There are also a number of application environment variables which can be used to locate tasks and project files or to enable specific features and a number of other general purpose variables are recognized if they are set in your environment.

Licensing Variables:

LM_LICENSE_FILE
MGLS_CONN_TIMEOUT
MGLS_HOME
MGLS_LICENSE_FILE
MGLS_PKGINFO_FILE

HDL Designer Series Variables:

HDS_DEBUGFONTS
HDS_GENRULES_SCRIPT
HDS_HOME
HDS_INSTANCE_LIMIT
HDS_KANJI_DIALOGS
HDS_KEEPFILE
HDS_KEYS
HDS_LIB_MIGRATION
HDS_LIBS
HDS_LOG_TIMEOUT
HDS_MAX_ILOG_AREA
HDS_NEW_PROJECT_DIR
HDS_PLUGINS
HDS_PORT
HDS_PREFS
HDS_PROJECT_DIR
HDS_REPOSITORY
HDS_SIGNAL_LIMIT
HDS_TCL
HDS_TEAM_HOME
HDS_TEAM_VER
HDS_TEAMPREFS
HDS_USER_HOME
HDS_USER_VER

General Purpose Variables:

CDS_INST_DIR
CVE_HOME
CVSROOT
EDITOR
EXEMPLAR
LD_LIBRARY_PATH
MGC_HOME
MGC_LOCATION_MAP
MGC_WD
MODELSIM
SPYGLASS_HOME
SSDIR
TZ

List of Variables

CDS_INST_DIR

Specifies a pathname to the location of a Cadence software tree. This variable can be used to specify the installation directory containing the Cadence NC-Sim simulator executable.

CVE_HOME

Specifies a pathname to the location of the Seamless CVE software. This location is required for library mapping when you instantiate a CVE model as an external HDL model in a block diagram.

CVSROOT

Specifies the pathname of a directory used as the repository for CVS source control objects (for example when setting up a CVS modules file outside the tool). It is set internally to the location specified in the version management options.

EDITOR

Specifies the default editor for text files on UNIX or Linux systems. It is usually set to the name of the editor and located using the default search path. This editor can be used for editing or viewing HDL text views files if you set **XTerm with Editor** as the text editor command in your preferences.

EXEMPLAR

Specifies a pathname to the installation directory containing the LeonardoSpectrum synthesis tools. This variable is not required when LeonardoSpectrum is invoked from a HDL Designer Series tool and may cause problems if set to an out-of-date location.

HDS_DEBUGFONTS

When set to any value, font mapping information is sent to standard error output.

HDS_GENRULES_SCRIPT

Specifies the pathname to a Tcl script used to expand view properties variables.

HDS_HOME

Specifies a pathname to the HDL Designer Series installation directory. This variable is used internally to locate application resources in the installation directory.

HDS_INSTANCE_LIMIT

Specifies a default integer limit to the number of instance declarations found in a HDL file by the HDL parser. The limit can be overidden by specifying a value in the **Checks** tab of the Main Settings dialog box.

HDS_KANJI_DIALOGS

When set to a non integer value, such as ‘ON’, enables a font which allows the entry of Kanji characters in the Comments dialog box.

Note

Setting the HDS_KANJI_DIALOGS to any non-integer value prevents the text from getting cut-off.

HDS_KEEPFILE

When set to any non zero value, the temporary list file created during HDL compilation is not deleted when the compilation window is closed.

HDS_KEYS

Specifies a pathname to an alternative location for the *hds.keys* file. If not set, a keys file in the wo is used (if it exists) or a keys file in your user directory. If not found in these locations, the default *hds.keys* file in the *resources/misc* installation subdirectory is used. This variable is ignored if the **-keysfile** command line switch is used to specify a keys file.

HDS_LIB_MIGRATION

When set to any value, the library migration wizard is available from the background popup menu in the project manager. This wizard can be used to migrate libraries created using pre-2003.1 releases to the hierarchical data model (HDM).

HDS_LIBS

Specifies the full pathname to the current user project file (*hds.hdp*). This variable is overridden if the location is specified using the -hdpfile command line switch.

HDS_LOG_TIMEOUT

Specifies a timeout period in seconds for the log displayer process. This variable is not usually required but can be used (set to a low value such as 5) to overcome a problem on Windows workstations which prevents the simulator from being re-invoked.

HDS_MAX_ILOG_AREA

Specifies the maximum image area in pixels which is used when exporting a diagram as HTML. If not set, defaults to 5000000 pixels square.

HDS_NEW_PROJECT_DIR

Specifies the pathname to the default location used to contain the folder for a new project.

HDS_PLUGINS

Specifies a list of pathnames to the location of directories containing "plug-in" drivers for external tools. Multiple locations can be specified by separating the pathname strings by a colon (on UNIX or Linux) or semi-colon (on a Windows PC). When set, a plug-in one of the specified directories takes priority over a standard plug-in with the same name in the *HDS_HOME\resources\downstream\drivers* directory.

HDS_PORT

Specifies an integer number for the IPC (inter-process communication) port used to communicate with an external tool. This variable should be set when you want to setup two-way communication between the HDL Designer Series source objects and HDL code displayed using a server application such as the GNU Emacs editor. Typically, HDS_PORT should be set to

<localhost>:<portnumber> where *localhost* is the name of your workstation and *portnumber* is an unused IPC port number or TCP service name allocated by your system administrator.

HDS_PREFS

Specifies the full pathname to a pre-2003.1 user preferences file (*.hdsPrefsV* where *V* is the software version number) which you want to be migrated to the latest release. This variable is overridden if the **-prefsfile** command line switch is used to specify the preferences file.

HDS_PROJECT_DIR

This variable is set internally to the location containing the folder for the active project. It can be used in the library mapping wizard to specify a root directory relative to the active project folder.

HDS_REPOSITORY

Specifies the pathname of a directory used as the repository for RCS source control objects. If this variable is set and no location is already set in your preferences, it is used as the RCS repository.

HDS_SIGNAL_LIMIT

Specifies a default integer limit to the number of signal declarations found in a HDL file by the HDL parser. The limit can be overidden by specifying a value in the **Checks** tab of the Main Settings dialog box.

HDS_TCL

Specifies the pathname of a Tcl script that is sourced at start up immediately before any file specified with the -do switch.

HDS_TEAM_HOME

Specifies a pathname to the location of the *hds_team* directory and sets team member mode. The *hds_team* directory contains the default shared resources project file (*shared.hdp)* and versioned files for team preferences, tasks and templates. The default location is in the user directory or the location from which team preferences for a previous release have been read. This variable is ignored in single-user mode or if an existing location is specified using the **-team_home** command line switch.

HDS_TEAM_VER

This variable is automatically derived at run time to specify the versioned directory containing team preference, task and template files for the current release. For example: *$HDS_TEAM_HOME/hds_team/v2003*

HDS_TEAMPREFS

Specifies the full pathname to a pre-2003.1 team preferences file (*.hdsTeamPrefsV* where *V* is the software version number) which you want to be migrated to the latest release. This variable is overridden if the -teamprefsfile command line switch is used to specify an old team preferences file.

HDS_USER_HOME

Specifies the location of the *hds_user* directory containing the user resource files (including versioned files for user preferences, tasks and templates). The default location is in the user

directory or in the location from which user preferences for a previous release have been read. This variable is ignored if an existing location is specified using the **-user_home** command line switch.

Note

If the user directory contains special characters, such as ü or ä, you should change the *hds_user* directory to another directory that does not contain any special characters.

HDS_USER_VER

This variable is automatically derived at run time to specify the versioned directory containing user preference, task and template files for the current release. For example: *$HDS_USER_HOME/hds_user/v2004*.

LD_LIBRARY_PATH

Specifies the location of directories containing some display libraries which are required on UNIX or Linux systems.

LM_LICENSE_FILE

Specifies the location of the licensing file. Typically specified by a port number and host name in the form: *<portnumber>@hostname* An evaluation license may be located by specifying the pathname. Multiple locations can be separated by a : (colon) on UNIX or Linux or by a ; (semi-colon) on Windows.

MGC_HOME

Specifies a pathname to the location of a Mentor Graphics software tree. This variable is not required but may be useful if you want to use other Mentor Graphics tools. (For example, if you want to read a default location map file in the MGC_HOME tree.)

MGC_LOCATION_MAP

Specifies a pathname to a Mentor Graphics location map file. When set, any valid location map entry can be used to set a library mapping pathname.

MGC_WD

Specifies a pathname to the location of the working directory used by the tools installed in a Mentor Graphics software tree. It is not used by the HDL Designer Series tools. However, if you use the ModelSim downstream tools, the *vmap* utility checks for an existing *modelsim.ini* file in this directory and if it exists, references this file for library mapping.

MGLS_CONN_TIMEOUT

Specifies a delay (in seconds) to wait for the license server to respond. The default is 10 but it can be increased to reduce the risk of timeout due to slow response from the server.

MGLS_HOME

Specifies a pathname to the location of the Mentor Graphics licensing system on a UNIX or Linux system.

MGLS_LICENSE_FILE

Specifies the location of an alternative license file that is used in preference to the LM_LICENSE_FILE variable for users who are already using other Mentor Graphics products.

MGLS_PKGINFO_FILE

Specifies a pathname to a directory containing an alternative *mgc.pkginfo* file which may be required in an existing UNIX MGC licensing environment. If this variable is not set, HDS uses the *mgc.pkginfo* file in the *bin* subdirectory of the HDS installation.

MODELSIM

Specifies a pathname to the initialization file (*modelsim.ini*) used by the ModelSim compiler and simulator on UNIX or Linux systems. HDL Designer Series tools create this file in the compiled library directory and the variable does not need to be set unless you invoke ModelSim independently.

SPYGLASS_HOME

Specifies a pathname to the location of a SpyGlass software tree containing the Atrenta SpyGlass RTL rule checker.

SSDIR

Specifies a pathname to the *srcsafe.ini* file in a Microsoft or Mainsoft Visual SourceSafe version control system.

TZ

Specifies the time zone. Usually set to an alphabetic time zone name. For example: GB

Setting Environment Variables

An environment variable is a shell-level variable that lets you communicate with your program and to set its internal states as it is executing. The names of these variables and the values that you assign to them are case sensitive.

Environment variables can be set on UNIX systems using the *set* or *setenv* shell commands. For example:

```
setenv HDS_REPOSITORY /usr1/hds_repository_directory
```

User and system environment variables can be set on Windows systems using the **Advanced** tab of the System dialog box which can be accessed from the Windows Control Panel. To enter a new user variable, check that no existing variable is selected and enter the new variable name and value. For example:

```
Variable: HDS_REPOSITORY
Value: C:\Designs\hds_repository_directory
```

Note

Take care that an existing system variable is not selected when using the dialog box. New user variables are available when you apply the dialog box but accidental changes to a system variable may cause problems later when rebooting your machine.

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End-User License Agreement

The latest version of the End-User License Agreement is available on-line at:
www.mentor.com/eula

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Rev. 100615, Part No. 246066